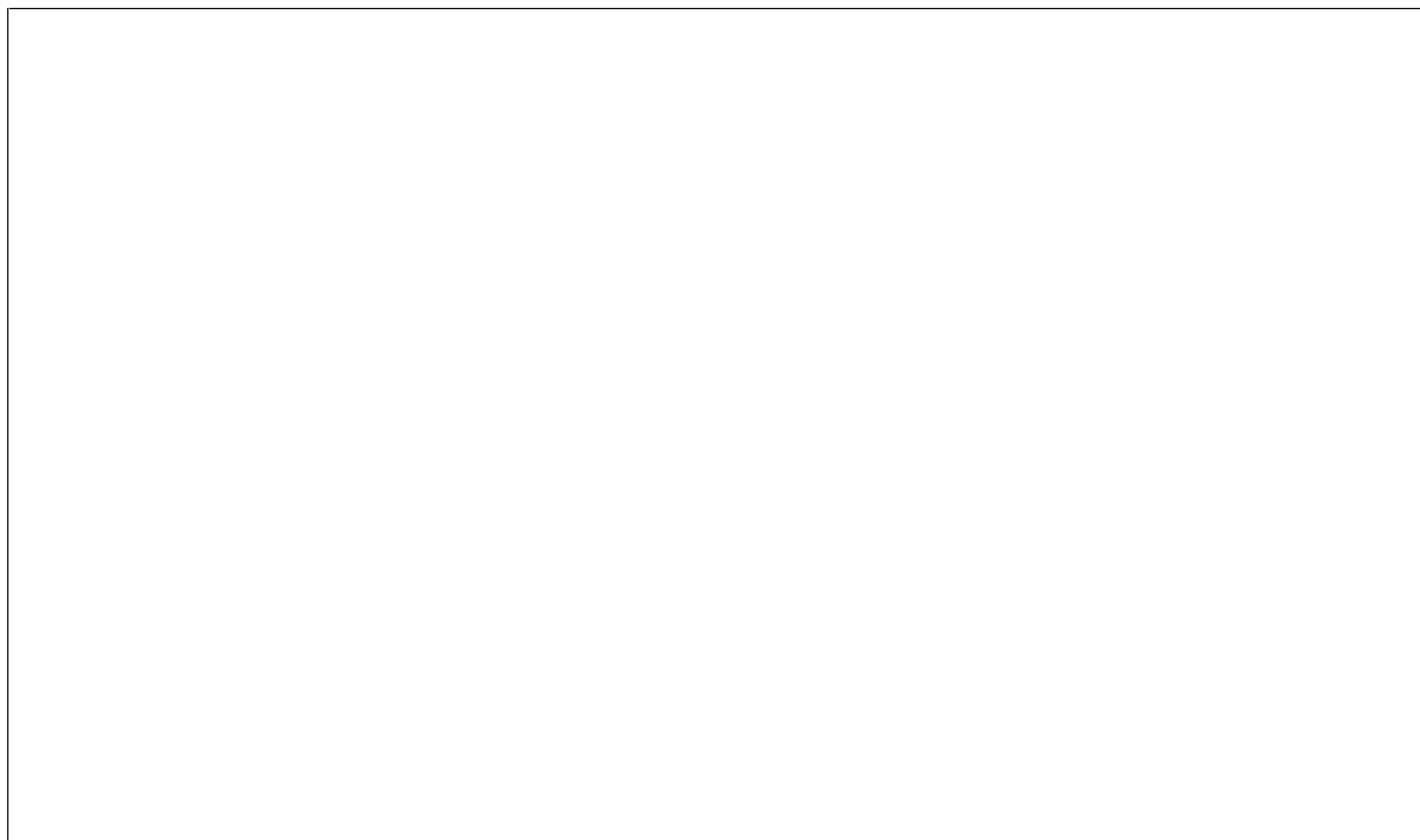


# SIEMENS



## Microcomputer Components

8-Bit CMOS Microcontroller

C501

Preliminary Data Sheet 08.95

<b>C501</b>	
<b>Revision History :</b>	<b>Current Version: 08.95</b>
Previous Releases:	03.95, 08.94, 11.93, 11.92
Page	Subjects (changes since last revision)
Several	SAB-C501 replaced by term C501
2, 3	Ordering information with notes are updated
26	$I_{CC}$ for idle mode corrected
31	permissible float time in note modified
34	$t_{PXIZ}$ and permissible float time in note modified
35	$t_{LLAX2}$ for variable clock corrected
42	Typical value of the two capacitors in crystal oscillator mode changed
44, 46, 48	Package information for "G" versions added

#### Edition 08.95

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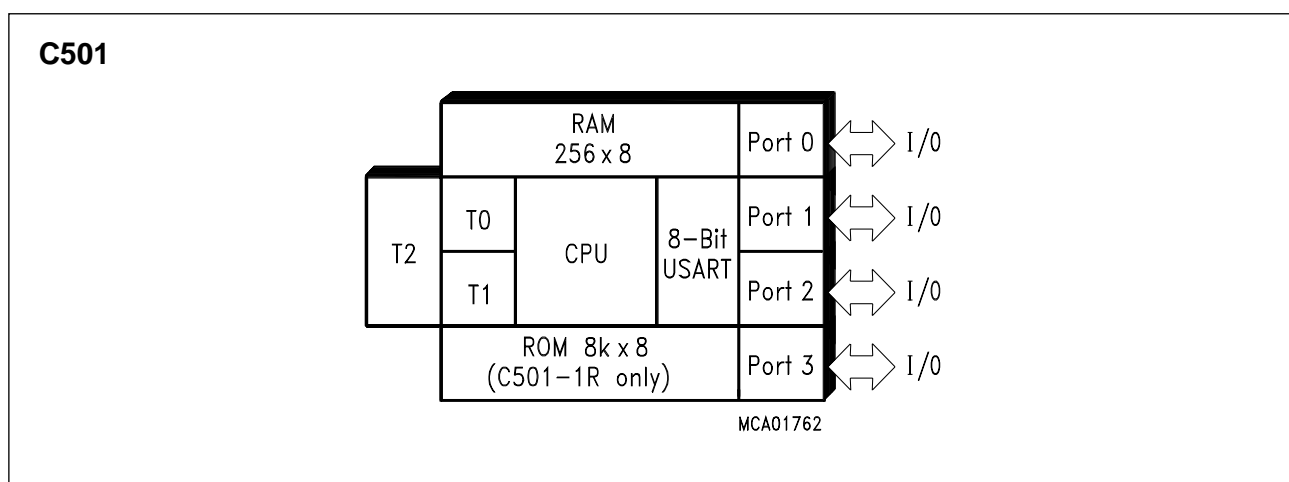
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### Preliminary

- Fully compatible to standard 8051 microcontroller
- Versions for 12/24/40 MHz operating frequency
- 8 K × 8 ROM (C501-1R only)
- 256 × 8 RAM
- Four 8-bit ports
- Three 16-bit Timers / Counters (Timer 2 with Up/Down Counter feature)
- USART
- Six interrupt sources, two priority levels
- Power Saving Modes
- P-DIP-40, P-LCC-44 package, and P-MQFP-44
- Temperature ranges:     SAB-C501             $T_A$ : 0 °C to 70 °C  
                                  SAF-C501             $T_A$ : - 40 °C to 85 °C



The C501-L/C501-1R described in this document is compatible with the SAB 80C32/C52 and can be used for all present SAB 80C52 applications.

The C501-1R contains a non-volatile 8 K × 8 read-only program memory, a volatile 256 × 8 read/write data memory, four ports, three 16-bit timers counters, a seven source, two priority level interrupt structure and a serial port. The C501-L is identical, except that it lacks the program memory on chip. Therefore, the term C501 refers to both versions within this specification unless otherwise noted. Further, the term C501 refers to all versions which are available in the different temperature ranges, marked with SAB-C501.... or SAF-C501.... .

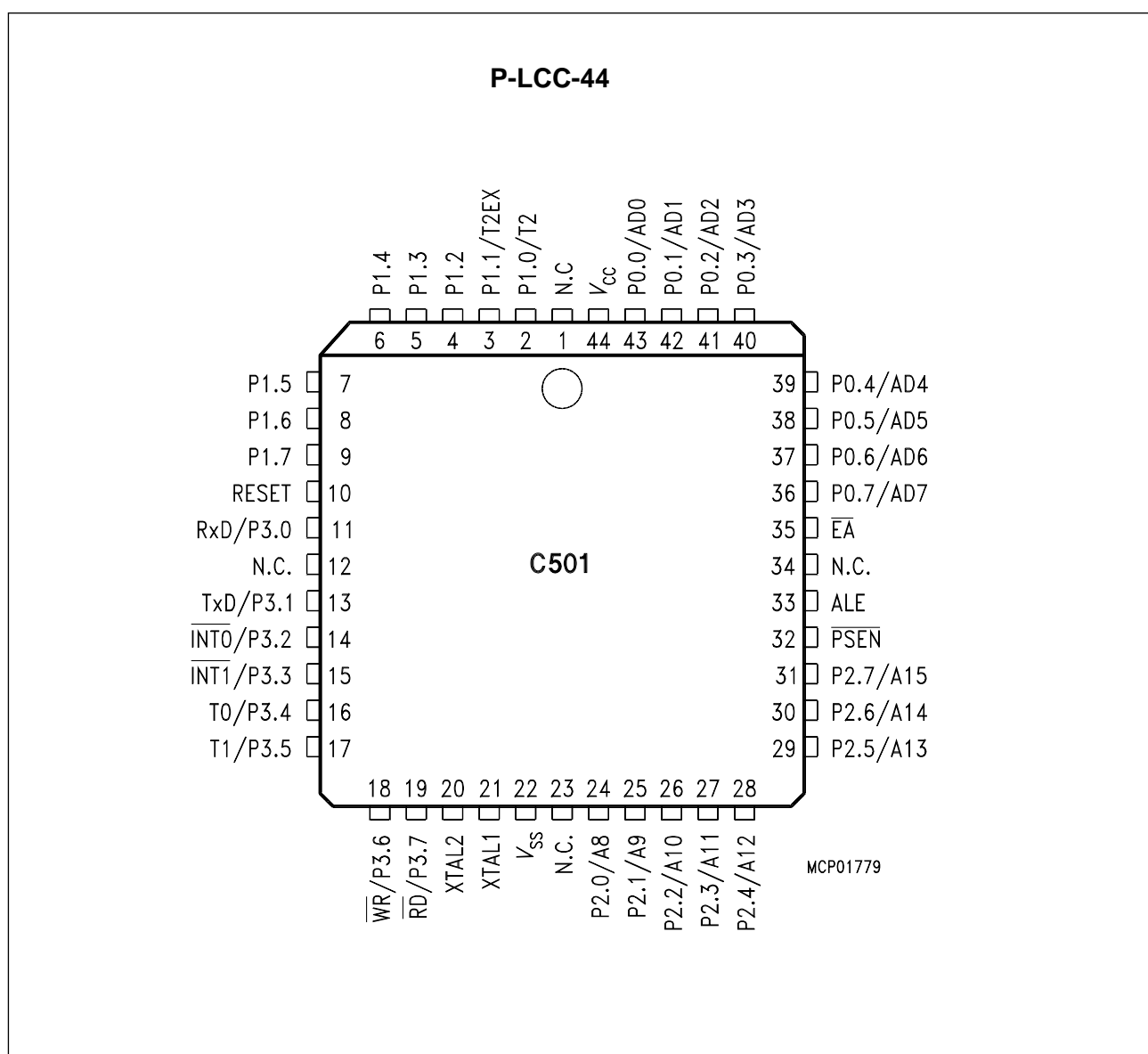
## Ordering Information

Type	Ordering Code	Package	Description (8-Bit CMOS microcontroller)
SAB-C501-LN SAB-C501-LP SAB-C501-LM SAB-C501G-LN SAB-C501G-LP SAB-C501G-LM	Q67120-C844 Q67120-C846 Q67120-C943 Q67120-C0969 Q67120-C0968 Q67126-C0970	P-LCC-44 P-DIP-40 P-MQFP-44 P-LCC-44 P-DIP-40 P-MQFP-44	for external memory (12 MHz)
SAB-C501G-1RN SAB-C501G-1RP SAB-C501G-1RM	Q67120-DXXX Q67120-DXXX Q67126-DXXX	P-LCC-44 P-DIP-40 P-MQFP-44	with mask-programmable ROM (12 MHz)
SAB-C501-L24N SAB-C501-L24P SAB-C501-L24M SAB-C501G-L24N SAB-C501G-L24P SAB-C501G-L24M	Q67120-C948 Q67120-C979 Q67120-C972 Q67120-C1001 Q67120-C0999 Q67126-C1014	P-LCC-44 P-DIP-40 P-MQFP-44 P-LCC-44 P-DIP-40 P-MQFP-44	for external memory (24 MHz)
SAB-C501G-1R24N SAB-C501G-1R24P SAB-C501G-1R24M	Q67120-DXXX Q67120-DXXX Q67126-DXXX	P-LCC-44 P-DIP-40 P-MQFP-44	with mask-programmable ROM (24 MHz)
SAB-C501-L40N SAB-C501-L40P SAB-C501-L40M SAB-C501G-L40N SAB-C501G-L40P SAB-C501G-L40M	Q67120-C867 Q67120-C868 Q67120-C947 Q67120-C1002 Q67120-C1000 Q67126-C1009	P-LCC-44 P-DIP-40 P-MQFP-44 P-LCC-44 P-DIP-40 P-MQFP-44	for external memory (40 MHz)
SAB-C501G-1R40N SAB-C501G-1R40P SAB-C501G-1R40M	Q67120-DXXX Q67120-DXXX Q67126-DXXX	P-LCC-44 P-DIP-40 P-MQFP-44	with mask-programmable ROM (40 MHz)
SAF-C501-LN SAF-C501-LP	Q67120-C845 Q67120-C847	P-LCC-44 P-DIP-40	for external memory (12 MHz) ext. temp. – 40 °C to 85 °C
SAF-C501-L40N SAF-C501-L40P	Q67120-C990 Q67120-C991	P-LCC-44 P-DIP-40	for external memory (40 MHz) ext. temp. – 40 °C to 85 °C

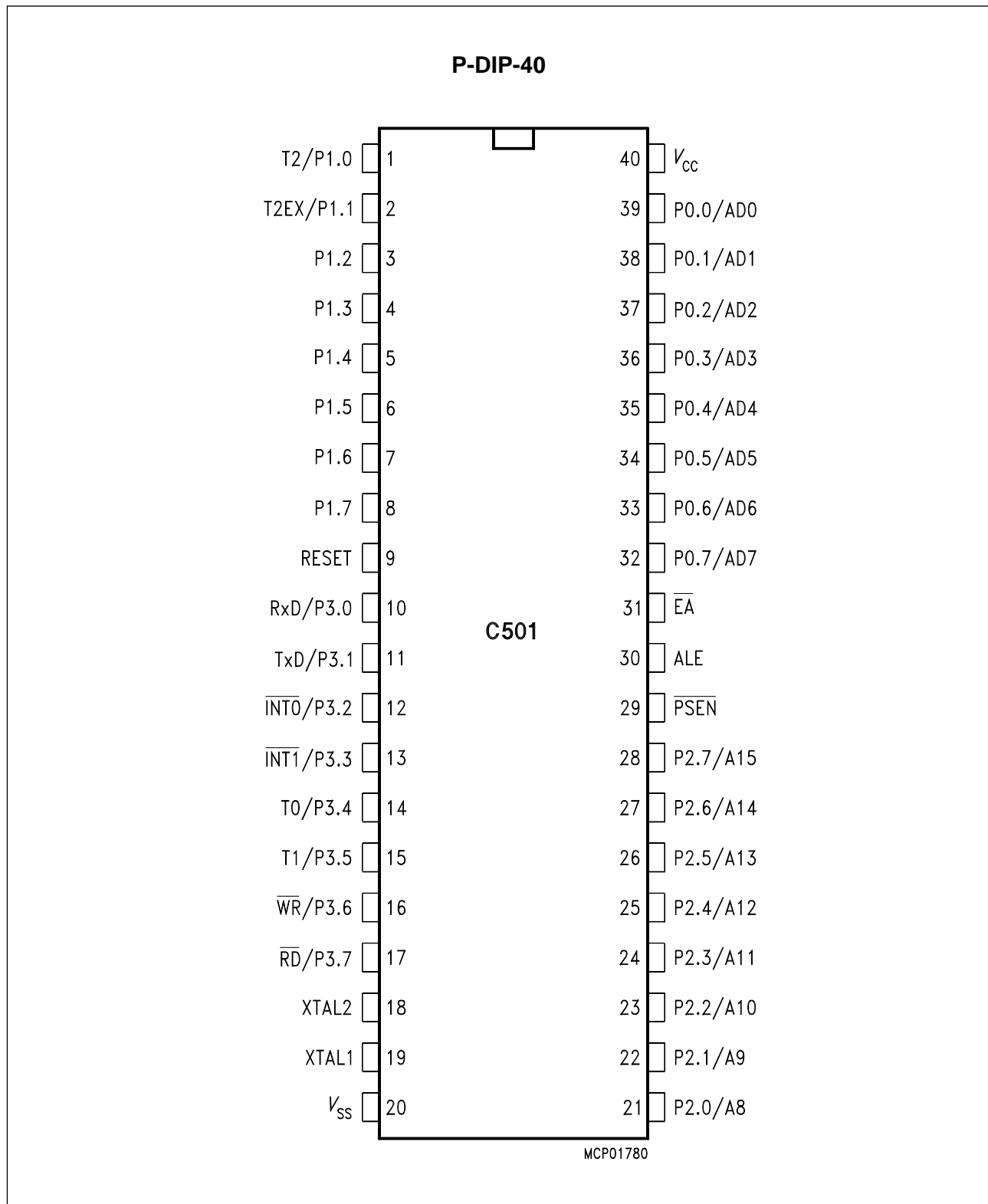
**Note:** Versions for extended temperature range – 40 °C to 110 °C (SAH-C501) on request.  
 The C501G versions are the latest steppings.  
 The C501 “non-G” versions are planned to be phased out.  
 The ordering number of ROM types (DXXXX extensions) is defined after program release (verification) of the customer.

## Pin Configuration

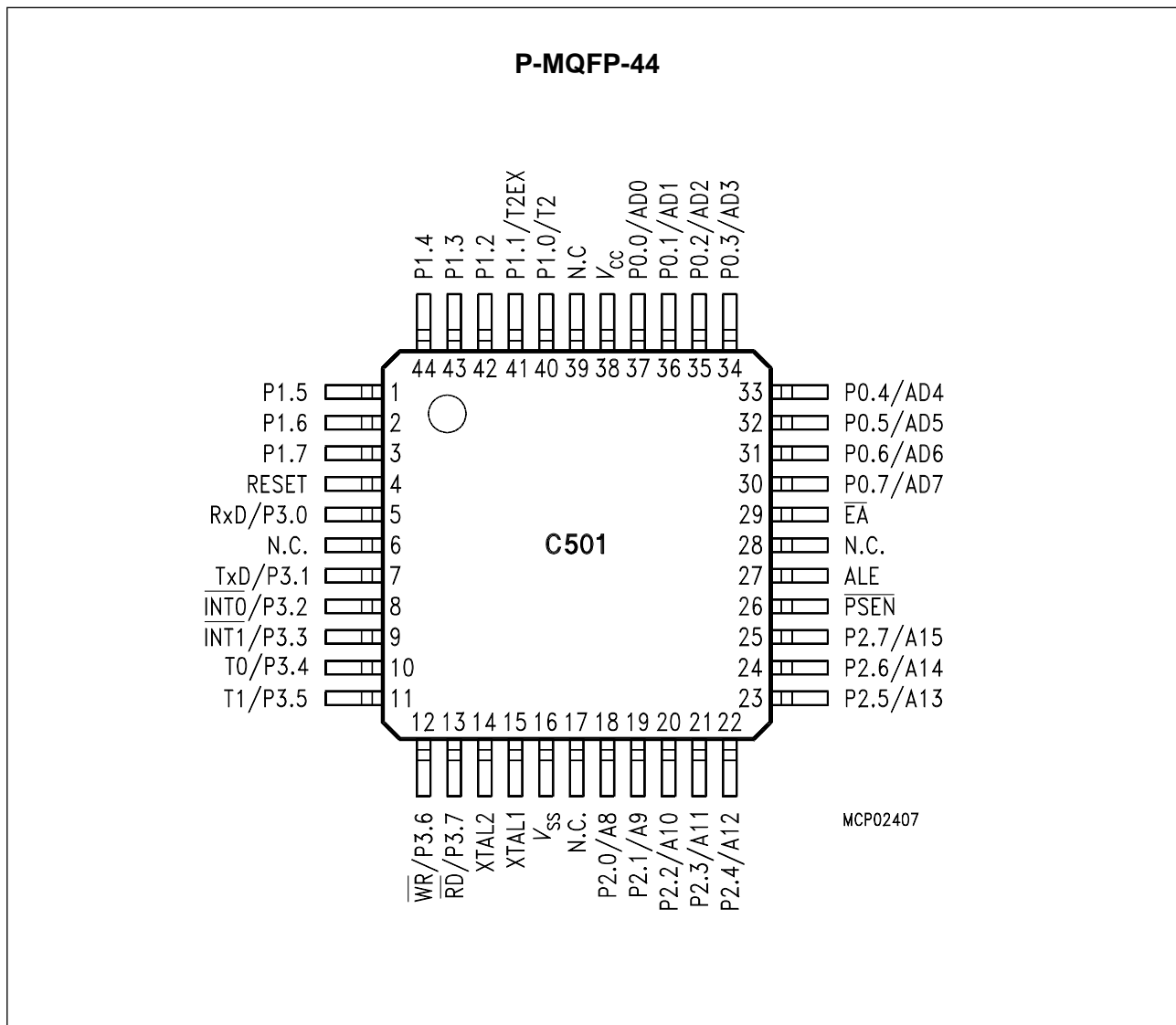
(top view)

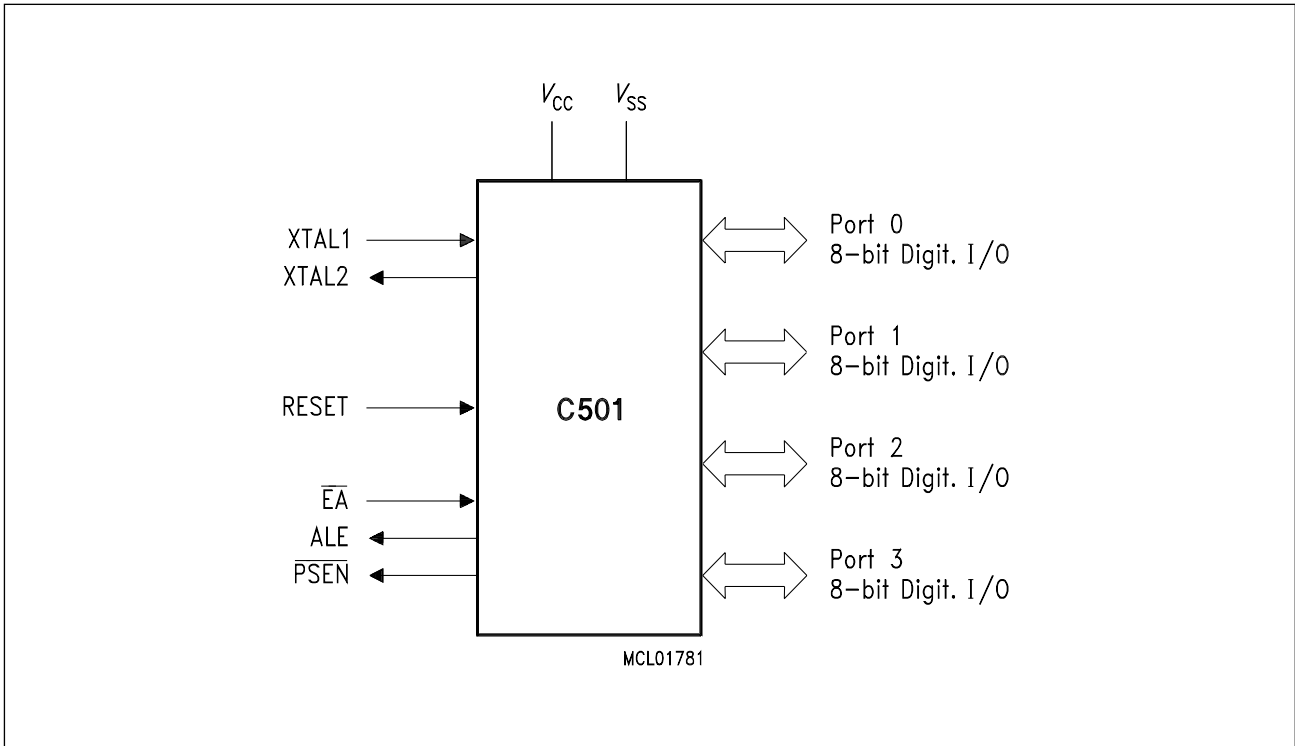


## Pin Configuration (top view)



## Pin Configuration (top view)





Logic Symbol

## Pin Definitions and Functions

Symbol	Pin Number			I/O <sup>1)</sup>	Function
	P-LCC-44	P-DIP-40	P-MQFP-44		
P1.0 – P1.7	2–9	1–8	40–44, 1–3,	I/O	<p><b>Port 1</b> is a bidirectional I/O port with internal pull-up resistors. Port 1 pins that have 1s written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 1 pins being externally pulled low will source current (<math>I_{IL}</math>, in the DC characteristics) because of the internal pull-up resistors. Port 1 also contains the timer 2 pins as secondary function. The output latch corresponding to a secondary function must be pro-grammed to a one (1) for that function to operate.</p> <p>The secondary functions are assigned to the pins of port 1, as follows:</p> <p>P1.0 T2 Input to counter 2 P1.1 T2EX Capture - Reload trigger of timer 2 / Up-Down count</p>
	2 3	1 2	40 41		

<sup>1)</sup> I = Input  
O = Output

## Pin Definitions and Functions (cont'd)

Symbol	Pin Number			I/O <sup>1)</sup>	Function
	P-LCC-44	P-DIP-40	P-MQFP-44		
P3.0 – P3.7	11, 13–19	10–17	5, 7–13	I/O	<p><b>Port 3</b> is a bidirectional I/O port with internal pull-up resistors. Port 3 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state they can be used as inputs. As inputs, port 3 pins being externally pulled low will source current (<math>I_{IL}</math>, in the DC characteristics) because of the internal pull-up resistors. Port 3 also contains the interrupt, timer, serial port 0 and external memory strobe pins which are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate.</p> <p>The secondary functions are assigned to the pins of port 3, as follows:</p> <p>P3.0 RxD receiver data input (asynchronous) or data input output (synchronous) of serial interface 0</p> <p>P3.1 TxD transmitter data output (asynchronous) or clock output (synchronous) of the serial interface 0</p> <p>P3.2 <math>\overline{INT0}</math> interrupt 0 input/timer 0 gate control</p> <p>P3.3 <math>\overline{INT1}</math> interrupt 1 input/timer 1 gate control</p> <p>P3.4 T0 counter 0 input</p> <p>P3.5 <math>\overline{T1}</math> counter 1 input</p> <p>P3.6 <math>\overline{WR}</math> the write control signal latches the data byte from port 0 into the external data memory</p> <p>P3.7 <math>\overline{RD}</math> the read control signal enables the external data memory to port 0</p>
	11	10	5		
	13	11	7		
	14	12	8		
	15	13	9		
	16	14	10		
	17	15	11		
	18	16	12		
	19	17	13		

\*) I = Input  
O = Output

## Pin Definitions and Functions (cont'd)

Symbol	Pin Number			I/O <sup>1)</sup>	Function
	P-LCC-44	P-DIP-40	P-MQFP-44		
XTAL2	20	18	14	–	<b>XTAL2</b> Output of the inverting oscillator amplifier.
XTAL1	21	19	15	–	<b>XTAL1</b> Input to the inverting oscillator amplifier and input to the internal clock generator circuits.  To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is divided down by a divide-by-two flip-flop. Minimum and maximum high and low times as well as rise fall times specified in the AC characteristics must be observed.
P2.0 – P2.7	24–31	21–28	18–25	I/O	<b>Port 2</b> is a bidirectional I/O port with internal pull-up resistors. Port 2 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state they can be used as inputs. As inputs, port 2 pins being externally pulled low will source current ( $I_{IL}$ , in the DC characteristics) because of the internal pull-up resistors. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pull-up resistors when issuing 1s. During accesses to external data memory that use 8-bit addresses (MOVX @Ri), port 2 issues the contents of the P2 special function register.

\*) I = Input  
O = Output

## Pin Definitions and Functions (cont'd)

Symbol	Pin Number			I/O <sup>1)</sup>	Function
	P-LCC-44	P-DIP-40	P-MQFP-44		
$\overline{\text{PSEN}}$	32	29	26	O	<b>The Program Store Enable</b> output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every six oscillator periods except during external data memory accesses. Remains high during internal program execution.
RESET	10	9	4	I	<b>RESET</b> A high level on this pin for two machine cycles while the oscillator is running resets the device. An internal diffused resistor to $V_{SS}$ permits power-on reset using only an external capacitor to $V_{CC}$ .
ALE	33	30	27	O	<b>The Address Latch Enable</b> output is used for latching the low-byte of the address into external memory during normal operation. It is activated every six oscillator periods except during an external data memory access.
$\overline{\text{EA}}$	35	31	29	I	<b>External Access Enable</b> When held at high level, instructions are fetched from the internal ROM (C501-1R only) when the PC is less than 2000 <sub>H</sub> . When held at low level, the C501 fetches all instructions from external program memory. For the C501-L this pin must be tied low.

\*) I = Input  
O = Output

## Pin Definitions and Functions (cont'd)

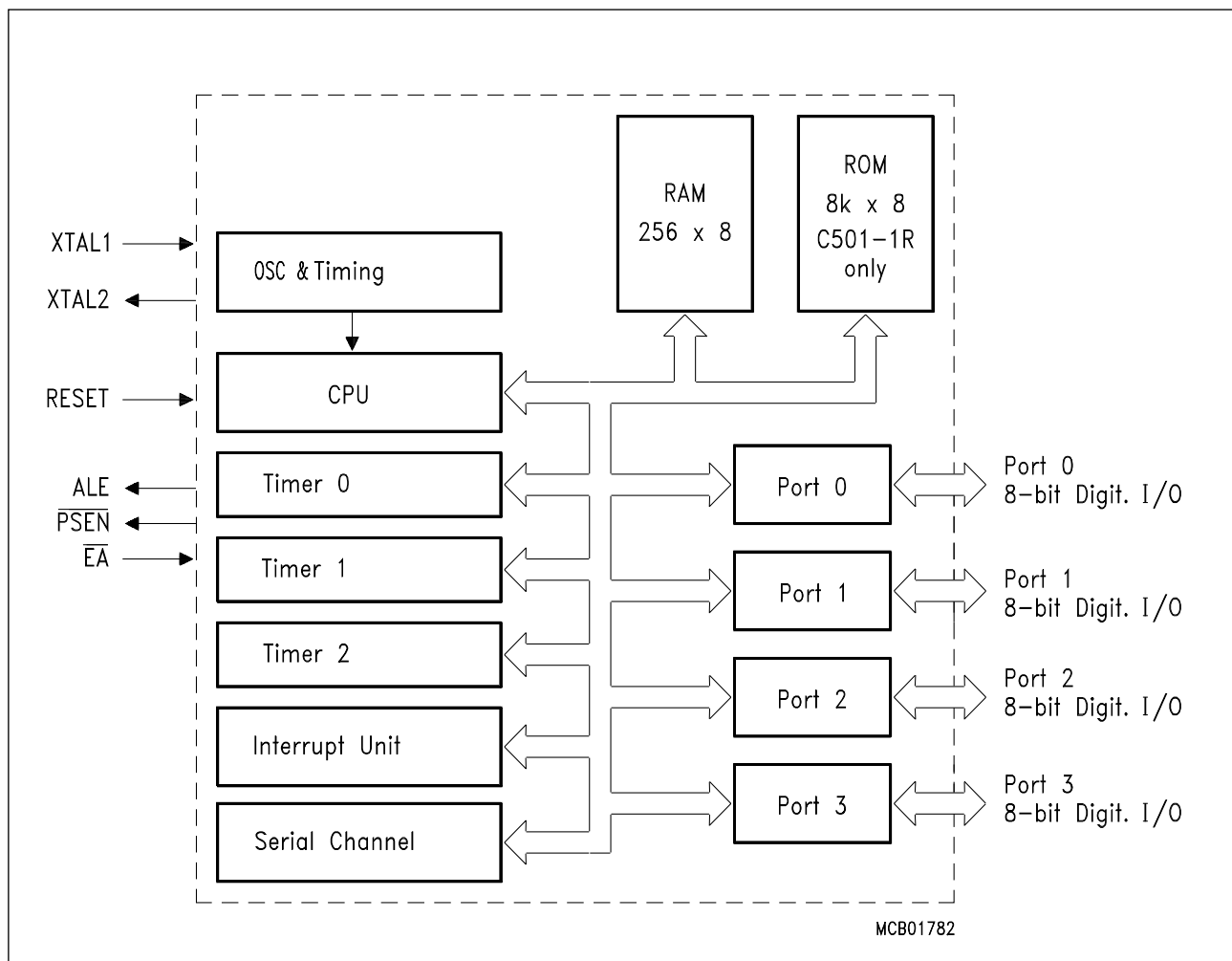
Symbol	Pin Number			I/O <sup>1)</sup>	Function
	P-LCC-44	P-DIP-40	P-MQFP-44		
P0.0 – P0.7	43–36	39–32	37–30	I/O	<p><b>Port 0</b> is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program or data memory. In this application it uses strong internal pull-up resistors when issuing 1s.</p> <p>Port 0 also outputs the code bytes during program verification in the C501-1R. External pull-up resistors are required during program verification.</p>
$V_{SS}$	22	20	16	–	<b>Circuit ground potential</b>
$V_{CC}$	44	40	38	–	<b>Supply terminal</b> for all operating modes
N.C.	1, 12, 23, 34	–	6, 17, 28, 39	–	<b>No connection</b>

## Functional Description

The C501 is fully compatible to the standard 8051 microcontroller family.

It is compatible with the SAB 80C52. While maintaining all architectural and operational characteristics of the SAB 80C52, the C501 incorporates some enhancements in the Timer2 Unit.

**Figure 1** shows a block diagram of the C501.



**Figure 1**  
**Block Diagram of the C501**

## CPU

The C501 is efficient both as a controller and as an arithmetic processor. It has extensive facilities for binary and BCD arithmetic and excels in its bit-handling capabilities. Efficient use of program memory results from an instruction set consisting of 44 % one-byte, 4 % two-byte, and 15 % three-byte instructions. With a 12 MHz crystal, 58 % of the instructions are executed in 1.0  $\mu$ s 24 MHz: 500 ns, 40 MHz: 300 ns).

## Special Function Register PSW

	MSB							LSB	
Bit No.	7	6	5	4	3	2	1	0	
Addr. D0 <sub>H</sub>	CY	AC	F0	RS1	RS0	OV	F1	P	PSW

Bit	Function
<b>CY</b>	<b>Carry Flag</b>
<b>AC</b>	<b>Auxiliary Carry Flag</b> (for BCD operations)
<b>F0</b>	<b>General Purpose Flag</b>
<b>RS1</b> <b>RS0</b>	<b>Register Bank select control bits</b>
0            0	Bank 0 selected, data address 00 <sub>H</sub> – 07 <sub>H</sub>
0            1	Bank 1 selected, data address 08 <sub>H</sub> – 0F <sub>H</sub>
1            0	Bank 2 selected, data address 10 <sub>H</sub> – 17 <sub>H</sub>
1            1	Bank 3 selected, data address 18 <sub>H</sub> – 1F <sub>H</sub>
<b>OV</b>	<b>Overflow Flag</b>
<b>F1</b>	<b>General Purpose Flag</b>
<b>P</b>	<b>Parity Flag</b> Set/cleared by hardware each instruction cycle to indicate an odd/even number of “one” bits in the accumulator, i.e. even parity.

Reset value of PSW is 00<sub>H</sub>.

## Special Function Registers

All registers, except the program counter and the four general purpose register banks, reside in the special function register area.

The 27 special function registers (SFR) include pointers and registers that provide an interface between the CPU and the other on-chip peripherals. There are also 128 directly addressable bits within the SFR area.

All SFRs are listed in **table 1**, **table 2**, and **table 3**.

In **table 1** they are organized in numeric order of their addresses. In **table 2** they are organized in groups which refer to the functional blocks of the C501. **Table 3** illustrates the contents of the SFRs.

**Table 1**  
**Special Function Registers in Numeric Order of their Addresses**

Address	Register	Contents after Reset	Address	Register	Contents after Reset
<b>80<sub>H</sub></b>	<b>P0</b> <sup>1)</sup>	<b>FF<sub>H</sub></b>	<b>98<sub>H</sub></b>	<b>SCON</b> <sup>1)</sup>	<b>00<sub>H</sub></b>
81 <sub>H</sub>	SP	07 <sub>H</sub>	99 <sub>H</sub>	SBUF	XX <sub>H</sub> <sup>2)</sup>
82 <sub>H</sub>	DPL	00 <sub>H</sub>	9A <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>
83 <sub>H</sub>	DPH	00 <sub>H</sub>	9B <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>
84 <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>	9C <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>
85 <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>	9D <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>
86 <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>	9E <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>
87 <sub>H</sub>	PCON	0XXX0000 <sub>B</sub> <sup>2)</sup>	9F <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>
<b>88<sub>H</sub></b>	<b>TCON</b> <sup>1)</sup>	<b>00<sub>H</sub></b>	<b>A0<sub>H</sub></b>	<b>P2</b> <sup>1)</sup>	<b>FF<sub>H</sub></b>
89 <sub>H</sub>	TMOD	00 <sub>H</sub>	A1 <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>
8A <sub>H</sub>	TL0	00 <sub>H</sub>	A2 <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>
8B <sub>H</sub>	TL1	00 <sub>H</sub>	A3 <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>
8C <sub>H</sub>	TH0	00 <sub>H</sub>	A4 <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>
8D <sub>H</sub>	TH1	00 <sub>H</sub>	A5 <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>
8E <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>	A6 <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>
8F <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>	A7 <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>
<b>90<sub>H</sub></b>	<b>P1</b> <sup>1)</sup>	<b>FF<sub>H</sub></b>	<b>A8<sub>H</sub></b>	<b>IE</b> <sup>1)</sup>	<b>0X000000<sub>B</sub></b> <sup>2)</sup>
91 <sub>H</sub>	reserved	00 <sub>H</sub>	A9 <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>
92 <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>	AA <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>
93 <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>	AB <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>
94 <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>	AC <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>
95 <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>	AD <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>
96 <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>	AE <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>
97 <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>	AF <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>

1) Bit-addressable Special Function Register

2) X means that the value is indeterminate and the location is reserved

**Table 1**  
**Special Function Registers in Numeric Order of their Addresses (cont'd)**

Address	Register	Contents after Reset	Address	Register	Contents after Reset
<b>B0<sub>H</sub></b>	<b>P3<sup>1)</sup></b>	<b>FF<sub>H</sub></b>	<b>D8<sub>H</sub></b>	reserved	XX <sub>H</sub> <sup>2)</sup>
B1 <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>	D9 <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>
B2 <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>	DA <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>
B3 <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>	DB <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>
B4 <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>	DC <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>
B5 <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>	DD <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>
N6 <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>	DE <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>
B7 <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>	DF <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>
<b>B8<sub>H</sub></b>	<b>IP<sup>1)</sup></b>	<b>XX000000<sub>B</sub><sup>2)</sup></b>	<b>E0<sub>H</sub></b>	<b>ACC<sup>1)</sup></b>	<b>00<sub>H</sub></b>
B9 <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>	E1 <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>
BA <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>	E2 <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>
BB <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>	E3 <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>
BC <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>	E4 <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>
BD <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>	E5 <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>
BE <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>	E6 <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>
BF <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>	E7 <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>
<b>C0<sub>H</sub></b>	reserved	XX <sub>H</sub> <sup>2)</sup>	<b>E8<sub>H</sub></b>	reserved	XX <sub>H</sub> <sup>2)</sup>
C1 <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>	E9 <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>
C2 <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>	EA <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>
C3 <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>	EB <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>
C4 <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>	EC <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>
C5 <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>	ED <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>
C6 <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>	EE <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>
C7 <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>	EF <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>
<b>C8<sub>H</sub></b>	<b>T2CON</b>	<b>00<sub>H</sub></b>	<b>F0<sub>H</sub></b>	<b>B<sup>1)</sup></b>	<b>00<sub>H</sub></b>
C9 <sub>H</sub>	T2MOD	XXXXXXXX0 <sub>B</sub> <sup>2)</sup>	F1 <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>
CA <sub>H</sub>	RC2L	00 <sub>H</sub>	F2 <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>
CB <sub>H</sub>	RC2H	00 <sub>H</sub>	F3 <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>
CC <sub>H</sub>	TL2	00 <sub>H</sub>	F4 <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>
CD <sub>H</sub>	TH2	00 <sub>H</sub>	F5 <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>
CE <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>	F6 <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>
CF <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>	F7 <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>
<b>D0<sub>H</sub></b>	<b>PSW<sup>1)</sup></b>	<b>00<sub>H</sub></b>	<b>F8<sub>H</sub></b>	reserved	XX <sub>H</sub> <sup>2)</sup>
D1 <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>	F9 <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>
D2 <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>	FA <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>
D3 <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>	FB <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>
D4 <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>	FC <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>
D5 <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>	FD <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>
D6 <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>	FE <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>
D7 <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>	FF <sub>H</sub>	reserved	XX <sub>H</sub> <sup>2)</sup>

<sup>1)</sup> Bit-addressable Special Function Register

<sup>2)</sup> X means that the value is indeterminate and the location is reserved

**Table 2**  
**Special Function Registers - Functional Blocks**

Block	Symbol	Name	Address	Contents after Reset
CPU	ACC	Accumulator	<b>E0H</b> <sup>1)</sup>	00H
	B	B-Register	<b>F0H</b> <sup>1)</sup>	00H
	DPH	Data Pointer, High Byte	83H	00H
	DPL	Data Pointer, Low Byte	82H	00H
	PSW	Program Status Word Register	<b>D0H</b> <sup>1)</sup>	00H
	SP	Stack Pointer	81H	07H
Interrupt System	IE	Interrupt Enable Register	<b>A8H</b> <sup>1)</sup>	0X000000B <sup>2)</sup>
	IP	Interrupt Priority Register	<b>B8H</b> <sup>1)</sup>	XX000000B <sup>2)</sup>
Ports	P0	Port 0	<b>80H</b> <sup>1)</sup>	FFH
	P1	Port 1	<b>90H</b> <sup>1)</sup>	XXH <sup>3)</sup>
	P2	Port 2	<b>A0H</b> <sup>1)</sup>	FFH
	P3	Port 3	<b>B0H</b> <sup>1)</sup>	FFH
Serial Channels	PCON <sup>2)</sup>	Power Control Register	87H	0XXX0000B <sup>2)</sup>
	SBUF	Serial Channel Buffer Reg.	99H	XXH <sup>3)</sup>
	SCON	Serial Channel 0 Control Reg.	<b>98H</b> <sup>1)</sup>	00H
Timer 0 / Timer 1	TCON	Timer 0/1 Control Register	<b>88H</b> <sup>1)</sup>	00H
	TH0	Timer 0, High Byte	8CH	00H
	TH1	Timer 1, High Byte	8DH	00H
	TL0	Timer 0, Low Byte	8AH	00H
	TL1	Timer 1, Low Byte	8BH	00H
	TMOD	Timer Mode Register	89H	00H
Timer 2	T2CON	Timer 2 Control Register	<b>C8H</b> <sup>1)</sup>	00H
	T2MOD	Timer 2 Mode Register	C9H	00H
	RC2H	Timer 2 Reload Capture Reg., High Byte	CBH	00H
	RC2L	Timer 2 Reload Capture Reg., Low Byte	CAH	00H
	TH2	Timer 2, High Byte	CDH	00H
	TL2	Timer 2, Low Byte	CCH	00H
Pow. Sav. Modes	PCON	Power Control Register	87H	0XXX0000B <sup>2)</sup>

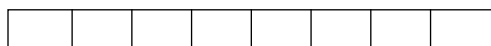
1) Bit-addressable special function registers

2) This special function register is listed repeatedly since some bits of it also belong to other functional blocks

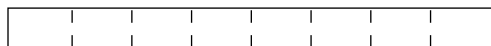
3) X means that the value is indeterminate and the location is reserved

**Table 3**  
**Contents of SFRs, SFRs in Numeric Order**

Address	Register	Bit 7	6	5	4	3	2	1	0
80 <sub>H</sub>	P0								
81 <sub>H</sub>	SP								
82 <sub>H</sub>	DPL								
83 <sub>H</sub>	DPH								
87 <sub>H</sub>	PCON	SMOD	–	–	–	GF1	GF0	PDE	IDLE
88 <sub>H</sub>	TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
89 <sub>H</sub>	TMOD	GATE	C/T	M1	M0	GATE	C/T	M1	M0
8A <sub>H</sub>	TL0								
8B <sub>H</sub>	TL1								
8C <sub>H</sub>	TH0								
8D <sub>H</sub>	TH1								
90 <sub>H</sub>	P1								
98 <sub>H</sub>	SCON	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
99 <sub>H</sub>	SBUF								
A0 <sub>H</sub>	P2								
A8 <sub>H</sub>	IE	EA	–	ET2	ES	ET1	EX1	ET0	EX0
B0 <sub>H</sub>	P3								
B8 <sub>H</sub>	IP	–	–	PT2	PS	PT1	PX1	PT0	PX0
C8 <sub>H</sub>	T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2
C9 <sub>H</sub>	T2MOD	–	–	–	–	–	–	–	DCEN



SFR bit and byte addressable



SFR not bit addressable

– : = this bit location is reserved

**Table 3**  
**Contents of SFRs, SFRs in Numeric Order (cont'd)**

Address	Register	Bit 7	6	5	4	3	2	1	0
CA <sub>H</sub>	RC2L								
CB <sub>H</sub>	RC2H								
CC <sub>H</sub>	TL2								
CD <sub>H</sub>	TH2								
D0 <sub>H</sub>	PSW	CY	AC	F0	RS1	RS0	OV	F1	P
E0 <sub>H</sub>	ACC								
F0 <sub>H</sub>	B								

--	--	--	--	--	--	--	--

 SFR bit and byte addressable

--	--	--	--	--	--	--	--

 SFR not bit addressable

– : = this bit location is reserved

**Timer / Counter 0 and 1**

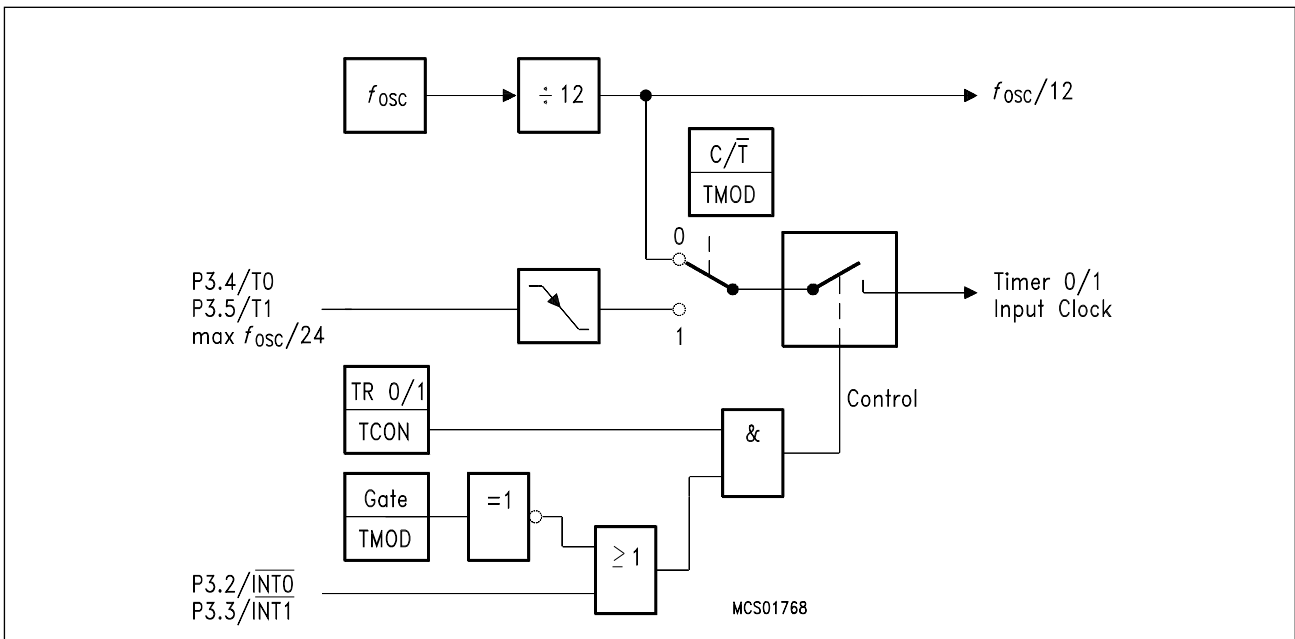
Timer/Counter 0 and 1 can be used in four operating modes as listed in **table 4**:

**Table 4**  
**Timer/Counter 0 and 1 Operating Modes**

Mode	Description	TMOD				Input Clock	
		Gate	C/T	M1	M0	internal	external (max)
0	8-bit timer/counter with a divide-by-32 prescaler	X	X	0	0	$f_{osc}/12 \times 32$	$f_{osc}/24 \times 32$
1	16-bit timer/counter	X	X	1	1	$f_{osc}/12$	$f_{osc}/24$
2	8-bit timer/counter with 8-bit autoreload	X	X	0	0	$f_{osc}/12$	$f_{osc}/24$
3	Timer/counter 0 used as one 8-bit timer/counter and one 8-bit timer Timer 1 stops	X	X	1	1	$f_{osc}/12$	$f_{osc}/24$

In the “timer” function (C/T = ‘0’) the register is incremented every machine cycle. Therefore the count rate is  $f_{osc}/12$ .

In the “counter” function the register is incremented in response to a 1-to-0 transition at its corresponding external input pin (P3.4/T0, P3.5/T1). Since it takes two machine cycles to detect a falling edge the max. count rate is  $f_{osc}/24$ . External inputs  $\overline{INT0}$  and  $\overline{INT1}$  (P3.2, P3.3) can be programmed to function as a gate to facilitate pulse width measurements. **Figure 2** illustrates the input clock logic.



**Figure 2**  
**Timer/Counter 0 and 1 Input Clock Logic**

## Timer 2

Timer 2 is a 16-bit Timer/Counter with an up/down count feature. It can operate either as timer or as an event counter which is selected by bit  $C/\overline{T2}$  (T2CON.1). It has three operating modes as shown in **table 5**.

**Table 5**  
**Timer/Counter 2 Operating Modes**

Mode	T2CON			T2MOD	T2CON	P1.1/ T2E X	Remarks	Input Clock	
	R×CLK or T×CLK	CP/ RL2	TR2	DCEN	EXEN			internal	external (P1.0/T2)
16-bit Auto- reload	0	0	1	0	0	X	reload upon overflow	$f_{osc}/12$	max $f_{osc}/24$
	0	0	1	0	1	↓	reload trigger (falling edge)		
	0	0	1	1	X	0	Down counting		
	0	0	1	1	X	1	Up counting		
16-bit Cap- ture	0	1	1	X	0	X	16 bit Timer/ Counter (only up-counting)	$f_{osc}/12$	max $f_{osc}/24$
	0	1	1	X	1	↓	capture TH2, TL2 → RC2H, RC2L		
Baud Rate Gene- rator	1	X	1	X	0	X	no overflow interrupt request (TF2)	$f_{osc}/2$	max $f_{osc}/24$
	1	X	1	X	1	↓	extra external interrupt ("Timer 2")		
off	X	X	0	X	X	X	Timer 2 stops	–	–

**Note:** ↓ =  falling edge

**Serial Interface (USART)**

The serial port is full duplex and can operate in four modes (one synchronous mode, three asynchronous modes) as illustrated in **table 6**. The possible baudrates can be calculated using the formulas given in **table 7**.

**Table 6**  
**USART Operating Modes**

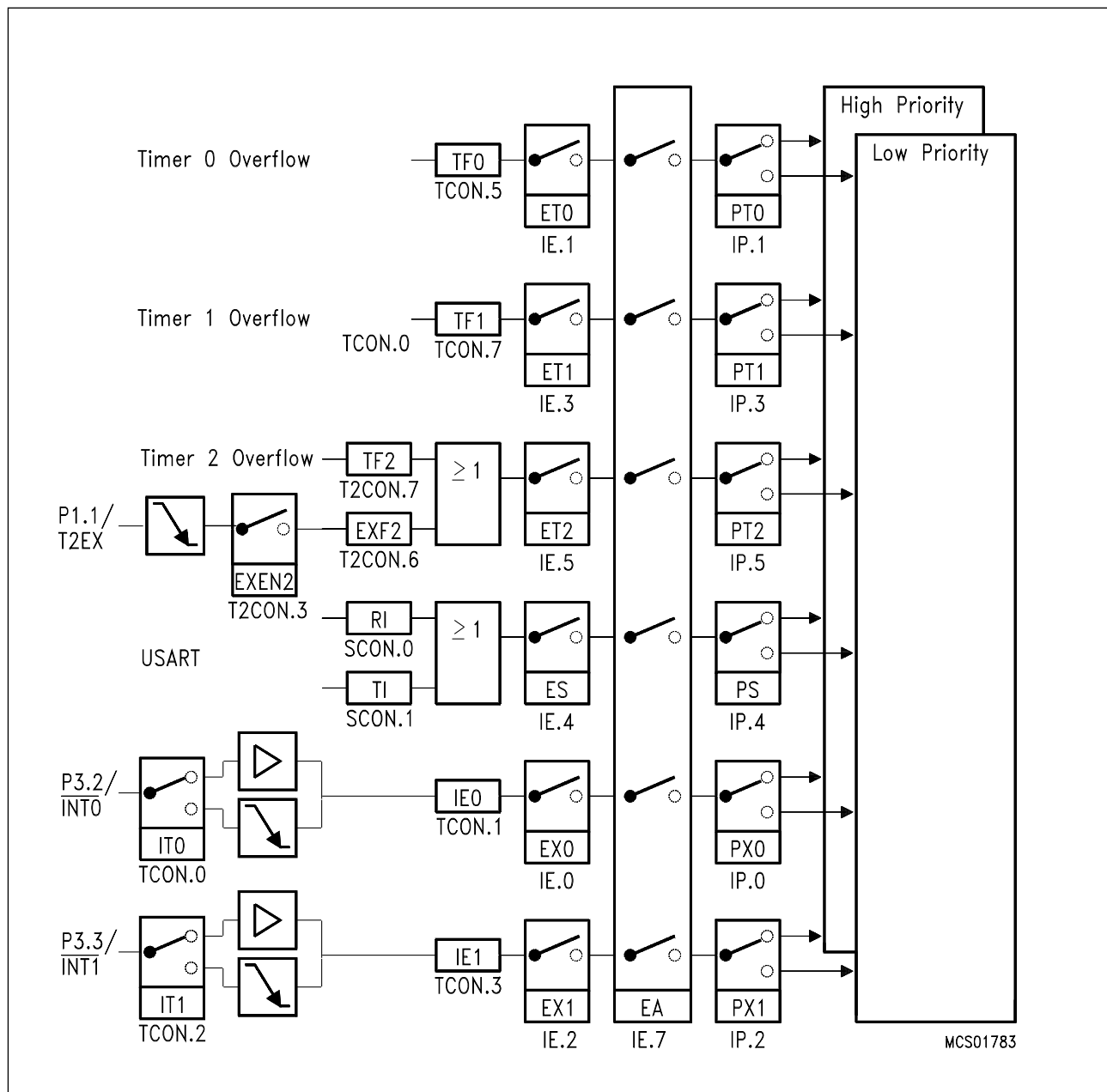
Mode	SCON		Baudrate	Description
	SM0	SM1		
0	0	0	$f_{osc}/12$	Serial data enters and exits through RxD. TxD outputs the shift clock. 8-bit are transmitted/received (LSB first)
1	0	1	Timer 1/2 overflow rate	8-bit UART 10 bits are transmitted (through TxD) or received (RxD)
2	1	0	$f_{osc}/32$ or $f_{osc}/64$	9-bit UART 11 bits are transmitted (TxD) or received (RxD)
3	1	1	Timer 1/2 overflow rate	9-bit UART Like mode 2 except the variable baud rate

**Table 7**  
**Formulas for Calculating Baudrates**

Baud Rate derived from	Interface Mode	Baudrate
Oscillator	0 2	$f_{osc}/12$ $(2^{SMOD} \times f_{osc}) / 64$
Timer 1 (16-bit timer) (8-bit timer with 8-bit autoreload)	1,3 1,3	$(2^{SMOD} \times \text{timer 1 overflow rate}) / 32$ $(2^{SMOD} \times f_{osc}) / (32 \times 12 \times (256 - TH1))$
Timer 2	1,3	$f_{osc} / (32 \times (65536 - (RC2H, RC2L)))$

**Interrupt System**

The C501 provides 6 interrupt sources with two priority levels. **Figure 3** gives a general overview of the interrupt sources and illustrates the request and control flags.



**Figure 3**  
**Interrupt Request Sources**

**Table 8**  
**Interrupt Sources and their Corresponding Interrupt Vectors**

Source (Request Flags)	Vector	Vector Address
IE0	External interrupt 0	0003 <sub>H</sub>
TF0	Timer 0 interrupt	000B <sub>H</sub>
IE1	External interrupt 1	0013 <sub>H</sub>
TF1	Timer 1 interrupt	001B <sub>H</sub>
RI + TI	Serial port interrupt	0023 <sub>H</sub>
TF2 + EXF2	Timer 2 interrupt	002B <sub>H</sub>

A low-priority interrupt can itself be interrupted by a high-priority interrupt, but not by another low-priority interrupt. A high-priority interrupt cannot be interrupted by any other interrupt source.

If two requests of different priority level are received simultaneously, the request of higher priority is serviced. If requests of the same priority are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence as shown in **table 9**.

**Table 9**  
**Interrupt Priority-Within-Level**

Interrupt Source		Priority
External Interrupt 0, Timer 0 Interrupt,	IE0 TF0	High
External Interrupt 1, Timer 1 Interrupt,	IE1 TF1	↓
Serial Channel, Timer 2 Interrupt,	RI + TI TF2 + EXF2	Low

## Power Saving Modes

Two power down modes are available, the Idle Mode and Power Down Mode.

The bits PDE and IDLE of the register PCON select the Power Down mode or the Idle mode, respectively. If the Power Down mode and the Idle mode are set at the same time, the Power Down mode takes precedence. **Table 10** gives a general overview of the power saving modes.

**Table 10**  
**Power Saving Modes Overview**

Mode	Entering Instruction Example	Leaving by	Remarks
Idle mode	ORL PCON, #01 <sub>H</sub>	– enabled interrupt – Hardware Reset	CPU is gated off CPU status registers maintain their data. Peripherals are active
Power-Down Mode	ORL PCON, #02 <sub>H</sub>	Hardware Reset	Oscillator is stopped, contents of on-chip RAM and SFR's are maintained (leaving Power Down Mode means redefinition of SFR contents).

In the Power Down mode of operation,  $V_{CC}$  can be reduced to minimize power consumption. It must be ensured, however, that  $V_{CC}$  is not reduced before the Power Down mode is invoked, and that  $V_{CC}$  is restored to its normal operating level, before the Power Down mode is terminated. The reset signal that terminates the Power Down mode also restarts the oscillator. The reset should not be activated before  $V_{CC}$  is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize (similar to power-on reset).

**Absolute Maximum Ratings**

Ambient temperature under bias ( $T_A$ ) .....	- 40 to + 85 °C
Storage temperature ( $T_{ST}$ ).....	- 65 to + 150 °C
Voltage on $V_{CC}$ pins with respect to ground ( $V_{SS}$ ) .....	- 0.5 V to 6.5 V
Voltage on any pin with respect to ground ( $V_{SS}$ ).....	- 0.5 V to $V_{CC} + 0.5$ V
Input current on any pin during overload condition.....	- 10 mA to + 10 mA
Absolute sum of all input currents during overload condition .....	100 mA
Power dissipation.....	TBD

**Note:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage of the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for longer periods may affect device reliability. During overload conditions ( $V_{IN} > V_{CC}$  or  $V_{IN} < V_{SS}$ ) the Voltage on  $V_{CC}$  pins with respect to ground ( $V_{SS}$ ) must not exceed the values defined by the absolute maximum ratings.

## DC Characteristics

$V_{CC} = 5\text{ V} + 10\%, -15\%$ ;  $V_{SS} = 0\text{ V}$ ;

$T_A = 0\text{ °C to }70\text{ °C}$  for the SAB-C501

$T_A = -40\text{ °C to }85\text{ °C}$  for the SAF-C501

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input low voltage (except $\overline{EA}$ , RESET)	$V_{IL}$	-0.5	$0.2 V_{CC} - 0.1$	V	-
Input low voltage ( $\overline{EA}$ )	$V_{IL1}$	-0.5	$0.2 V_{CC} - 0.3$	V	-
Input low voltage (RESET)	$V_{IL2}$	-0.5	$0.2 V_{CC} + 0.1$	V	-
Input high voltage (except XTAL1, $\overline{EA}$ , RESET)	$V_{IH}$	$0.2 V_{CC} + 0.9$	$V_{CC} + 0.5$	V	-
Input high voltage to XTAL1	$V_{IH1}$	$0.7 V_{CC}$	$V_{CC} + 0.5$	V	-
Input high voltage to $\overline{EA}$ , RESET	$V_{IH2}$	$0.6 V_{CC}$	$V_{CC} + 0.5$	V	-
Output low voltage (ports 1, 2, 3)	$V_{OL}$	-	0.45	V	$I_{OL} = 1.6\text{ mA}^{1)}$
Output low voltage (port 0, ALE, $\overline{PSEN}$ )	$V_{OL1}$	-	0.45	V	$I_{OL} = 3.2\text{ mA}^{1)}$
Output high voltage (ports 1, 2, 3)	$V_{OH}$	2.4 $0.9 V_{CC}$	- -	V	$I_{OH} = -80\text{ }\mu\text{A}$ , $I_{OH} = -10\text{ }\mu\text{A}$
Output high voltage (port 0 in external bus mode, ALE, $\overline{PSEN}$ )	$V_{OH1}$	2.4 $0.9 V_{CC}$	- -	V	$I_{OH} = -800\text{ }\mu\text{A}^{2)}$ , $I_{OH} = -80\text{ }\mu\text{A}^{2)}$
Logic 0 input current (ports 1, 2, 3)	$I_{IL}$	-10	-50	$\mu\text{A}$	$V_{IN} = 0.45\text{ V}$
Logical 1-to-0 transition current (ports 1, 2, 3)	$I_{TL}$	-65	-650	$\mu\text{A}$	$V_{IN} = 2\text{ V}$
Input leakage current (port 0, $\overline{EA}$ )	$I_{LI}$	-	$\pm 1$	$\mu\text{A}$	$0.45 < V_{IN} < V_{CC}$
Pin capacitance	$C_{IO}$	-	10	pF	$f_C = 1\text{ MHz}$ , $T_A = 25\text{ °C}$
Power supply current:					
Active mode, 12 MHz <sup>7)</sup>	$I_{CC}$	-	21	mA	$V_{CC} = 5\text{ V}$ , <sup>4)</sup>
Idle mode, 12 MHz <sup>7)</sup>	$I_{CC}$	-	4.8	mA	$V_{CC} = 5\text{ V}$ , <sup>5)</sup>
Active mode, 24 MHz <sup>7)</sup>	$I_{CC}$	-	36.2	mA	$V_{CC} = 5\text{ V}$ , <sup>4)</sup>
Idle mode, 24 MHz <sup>7)</sup>	$I_{CC}$	-	8.2	mA	$V_{CC} = 5\text{ V}$ , <sup>5)</sup>
Active mode, 40 MHz <sup>7)</sup>	$I_{CC}$	-	56.5	mA	$V_{CC} = 5\text{ V}$ , <sup>4)</sup>
Idle mode, 40 MHz <sup>7)</sup>	$I_{CC}$	-	12.7	mA	$V_{CC} = 5\text{ V}$ , <sup>5)</sup>
Power Down Mode	$I_{PD}$	-	50	$\mu\text{A}$	$V_{CC} = 2 \dots 5.5\text{ V}^{3)}$

- 1) Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the  $V_{OL}$  of ALE and port 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operation. In the worst case (capacitive loading > 100 pF), the noise pulse on ALE line may exceed 0.8 V. In such cases it may be desirable to qualify ALE with a schmitt-trigger, or use an address latch with a schmitt-trigger strobe input.
- 2) Capacitive loading on ports 0 and 2 may cause the  $V_{OH}$  on ALE and  $\overline{PSEN}$  to momentarily fall below the 0.9  $V_{CC}$  specification when the address lines are stabilizing.
- 3)  $I_{PD}$  (Power Down Mode) is measured under following conditions:  
 $\overline{EA} = \text{Port0} = V_{CC}$ ;  $\text{RESET} = V_{SS}$ ;  $\text{XTAL2} = \text{N.C.}$ ;  $\text{XTAL1} = V_{SS}$ ; all other pins are disconnected.
- 4)  $I_{CC}$  (active mode) is measured with:  
 $\text{XTAL1}$  driven with  $t_{CLCH}$ ,  $t_{CHCL} = 5 \text{ ns}$ ,  $V_{IL} = V_{SS} + 0.5 \text{ V}$ ,  $V_{IH} = V_{CC} - 0.5 \text{ V}$ ;  $\text{XTAL2} = \text{N.C.}$ ;  
 $\overline{EA} = \text{Port0} = \text{RESET} = V_{CC}$ ; all other pins are disconnected.  $I_{CC}$  would be slightly higher if a crystal oscillator is used (appr. 1 mA).
- 5)  $I_{CC}$  (Idle mode) is measured with all output pins disconnected and with all peripherals disabled;  
 $\text{XTAL1}$  driven with  $t_{CLCH}$ ,  $t_{CHCL} = 5 \text{ ns}$ ,  $V_{IL} = V_{SS} + 0.5 \text{ V}$ ,  $V_{IH} = V_{CC} - 0.5 \text{ V}$ ;  $\text{XTAL2} = \text{N.C.}$ ;  
 $\text{RESET} = \overline{EA} = V_{SS}$ ;  $\text{Port0} = V_{CC}$ ; all other pins are disconnected;
- 7)  $I_{CC \text{ max}}$  at other frequencies is given by:  
 active mode:  $I_{CC} = 1.27 \times f_{OSC} + 5.73$   
 idle mode:  $I_{CC} = 0.28 \times f_{OSC} + 1.45$   
 where  $f_{OSC}$  is the oscillator frequency in MHz.  $I_{CC}$  values are given in mA and measured at  $V_{CC} = 5 \text{ V}$ .

## AC Characteristics for C501-L / C501-1R

$V_{CC} = 5\text{ V} + 10\%, -15\%$ ;  $V_{SS} = 0\text{ V}$

$T_A = 0\text{ }^\circ\text{C}$  to  $70\text{ }^\circ\text{C}$  for the SAB-C501

$T_A = -40\text{ }^\circ\text{C}$  to  $85\text{ }^\circ\text{C}$  for the SAF-C501

( $C_L$  for port 0, ALE and  $\overline{\text{PSEN}}$  outputs = 100 pF;  $C_L$  for all other outputs = 80 pF)

## Program Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		12 MHz Clock		Variable Clock $1/t_{\text{CLCL}} = 3.5\text{ MHz to }12\text{ MHz}$		
		min.	max.	min.	max.	
ALE pulse width	$t_{\text{LHLL}}$	127	–	$2 t_{\text{CLCL}} - 40$	–	ns
Address setup to ALE	$t_{\text{AVLL}}$	43	–	$t_{\text{CLCL}} - 40$	–	ns
Address hold after ALE	$t_{\text{LLAX}}$	30	–	$t_{\text{CLCL}} - 53$	–	ns
ALE low to valid instr in	$t_{\text{LLIV}}$	–	233	–	$4 t_{\text{CLCL}} - 100$	ns
ALE to $\overline{\text{PSEN}}$	$t_{\text{LLPL}}$	58	–	$t_{\text{CLCL}} - 25$	–	ns
$\overline{\text{PSEN}}$ pulse width	$t_{\text{PLPH}}$	215	–	$3t_{\text{CLCL}} - 35$	–	ns
$\overline{\text{PSEN}}$ to valid instr in	$t_{\text{PLIV}}$	–	150	–	$3 t_{\text{CLCL}} - 100$	ns
Input instruction hold after $\overline{\text{PSEN}}$	$t_{\text{PXIX}}$	0	–	0	–	ns
Input instruction float after $\overline{\text{PSEN}}$	$t_{\text{PXIZ}}^*)$	–	63	–	$t_{\text{CLCL}} - 20$	ns
Address valid after $\overline{\text{PSEN}}$	$t_{\text{PXAV}}^*)$	75	–	$t_{\text{CLCL}} - 8$	–	ns
Address to valid instr in	$t_{\text{AVIV}}$	–	302	–	$5 t_{\text{CLCL}} - 115$	ns
Address float to $\overline{\text{PSEN}}$	$t_{\text{AZPL}}$	0	–	0	–	ns

\*) Interfacing the C501 to devices with float times up to 75 ns is permissible. This limited bus contention will not cause any damage to port 0 Drivers.

## AC Characteristics for C501-L / C501-1R (cont'd)

### External Data Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		12 MHz Clock		Variable Clock $1/t_{CLCL} = 3.5 \text{ MHz to } 12 \text{ MHz}$		
		min.	max.	min.	max.	
$\overline{\text{RD}}$ pulse width	$t_{RLRH}$	400	–	$6t_{CLCL} - 100$	–	ns
$\overline{\text{WR}}$ pulse width	$t_{WLWH}$	400	–	$6t_{CLCL} - 100$	–	ns
Address hold after ALE	$t_{LLAX2}$	30	–	$t_{CLCL} - 53$	–	ns
$\overline{\text{RD}}$ to valid data in	$t_{RLDV}$	–	252	–	$5t_{CLCL} - 165$	ns
Data hold after $\overline{\text{RD}}$	$t_{RHDX}$	0	–	0	–	ns
Data float after $\overline{\text{RD}}$	$t_{RHDZ}$	–	97	–	$2t_{CLCL} - 70$	ns
ALE to valid data in	$t_{LLDV}$	–	517	–	$8t_{CLCL} - 150$	ns
Address to valid data in	$t_{AVDV}$	–	585	–	$9t_{CLCL} - 165$	ns
ALE to $\overline{\text{WR}}$ or $\overline{\text{RD}}$	$t_{LLWL}$	200	300	$3t_{CLCL} - 50$	$3t_{CLCL} + 50$	ns
Address valid to $\overline{\text{WR}}$ or $\overline{\text{RD}}$	$t_{AVWL}$	203	–	$4t_{CLCL} - 130$	–	ns
$\overline{\text{WR}}$ or $\overline{\text{RD}}$ high to ALE high	$t_{WHLH}$	43	123	$t_{CLCL} - 40$	$t_{CLCL} + 40$	ns
Data valid to $\overline{\text{WR}}$ transition	$t_{QVWX}$	33	–	$t_{CLCL} - 50$	–	ns
Data setup before $\overline{\text{WR}}$	$t_{QVWH}$	433	–	$7t_{CLCL} - 150$	–	ns
Data hold after $\overline{\text{WR}}$	$t_{WHQX}$	33	–	$t_{CLCL} - 50$	–	ns
Address float after $\overline{\text{RD}}$	$t_{RLAZ}$	–	0	–	0	ns

## AC Characteristics for C501-L24 / C501-1R24 (cont'd)

### External Clock Drive Characteristics

Parameter	Symbol	Limit Values		Unit
		Variable Clock Freq. = 3.5 MHz to 12 MHz		
		min.	max.	
Oscillator period	$t_{CLCL}$	83.3	285.7	ns
High time	$t_{CHCX}$	20	$t_{CLCL} - t_{CLCX}$	ns
Low time	$t_{CLCX}$	20	$t_{CLCL} - t_{CHCX}$	ns
Rise time	$t_{CLCH}$	–	20	ns
Fall time	$t_{CHCL}$	–	20	ns

### AC Characteristics for C501-L24 / C501-1R24

$V_{CC} = 5\text{ V} + 10\%, -15\%$ ;  $V_{SS} = 0\text{ V}$

$T_A = 0\text{ °C}$  to  $70\text{ °C}$  for the SAB-C501

( $C_L$  for port 0, ALE and  $\overline{\text{PSEN}}$  outputs = 100 pF;  $C_L$  for all other outputs = 80 pF)

### Program Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		24 MHz Clock		Variable Clock $1/t_{\text{CLCL}} = 3.5\text{ MHz to }24\text{ MHz}$		
		min.	max.	min.	max.	
ALE pulse width	$t_{\text{LHLL}}$	43	–	$2 t_{\text{CLCL}} - 40$	–	ns
Address setup to ALE	$t_{\text{AVLL}}$	17	–	$t_{\text{CLCL}} - 25$	–	ns
Address hold after ALE	$t_{\text{LLAX}}$	17	–	$t_{\text{CLCL}} - 25$	–	ns
ALE low to valid instr in	$t_{\text{LLIV}}$	–	80	–	$4 t_{\text{CLCL}} - 87$	ns
ALE to $\overline{\text{PSEN}}$	$t_{\text{LLPL}}$	22	–	$t_{\text{CLCL}} - 20$	–	ns
$\overline{\text{PSEN}}$ pulse width	$t_{\text{PLPH}}$	95	–	$3 t_{\text{CLCL}} - 30$	–	ns
$\overline{\text{PSEN}}$ to valid instr in	$t_{\text{PLIV}}$	–	60	–	$3 t_{\text{CLCL}} - 65$	ns
Input instruction hold after $\overline{\text{PSEN}}$	$t_{\text{PXIX}}$	0	–	0	–	ns
Input instruction float after $\overline{\text{PSEN}}$	$t_{\text{PXIZ}}^*)$	–	32	–	$t_{\text{CLCL}} - 10$	ns
Address valid after $\overline{\text{PSEN}}$	$t_{\text{PXAV}}^*)$	37	–	$t_{\text{CLCL}} - 5$	–	ns
Address to valid instr in	$t_{\text{AVIV}}$	–	148	–	$5 t_{\text{CLCL}} - 60$	ns
Address float to $\overline{\text{PSEN}}$	$t_{\text{AZPL}}$	0	–	0	–	ns

\*) Interfacing the C501 to devices with float times up to 37 ns is permissible. This limited bus contention will not cause any damage to port 0 Drivers.

## AC Characteristics for C501-L24 / C501-1R24 (cont'd)

### External Data Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		24 MHz Clock		Variable Clock $1/t_{\text{CLCL}} = 3.5 \text{ MHz to } 24 \text{ MHz}$		
		min.	max.	min.	max.	
$\overline{\text{RD}}$ pulse width	$t_{\text{RLRH}}$	180	–	$6 t_{\text{CLCL}} - 70$	–	ns
$\overline{\text{WR}}$ pulse width	$t_{\text{WLWH}}$	180	–	$6 t_{\text{CLCL}} - 70$	–	ns
Address hold after ALE	$t_{\text{LLAX2}}$	15	–	$t_{\text{CLCL}} - 27$	–	ns
$\overline{\text{RD}}$ to valid data in	$t_{\text{RLDV}}$	–	118	–	$5 t_{\text{CLCL}} - 90$	ns
Data hold after $\overline{\text{RD}}$	$t_{\text{RHDX}}$	0	–	0	–	ns
Data float after $\overline{\text{RD}}$	$t_{\text{RHDZ}}$	–	63	–	$2 t_{\text{CLCL}} - 20$	ns
ALE to valid data in	$t_{\text{LLDV}}$	–	200	–	$8 t_{\text{CLCL}} - 133$	ns
Address to valid data in	$t_{\text{AVDV}}$	–	220	–	$9 t_{\text{CLCL}} - 155$	ns
ALE to $\overline{\text{WR}}$ or $\overline{\text{RD}}$	$t_{\text{LLWL}}$	75	175	$3 t_{\text{CLCL}} - 50$	$3 t_{\text{CLCL}} + 50$	ns
Address valid to $\overline{\text{WR}}$ or $\overline{\text{RD}}$	$t_{\text{AVWL}}$	67	–	$4 t_{\text{CLCL}} - 97$	–	ns
$\overline{\text{WR}}$ or $\overline{\text{RD}}$ high to ALE high	$t_{\text{WHLH}}$	17	67	$t_{\text{CLCL}} - 25$	$t_{\text{CLCL}} + 25$	ns
Data valid to $\overline{\text{WR}}$ transition	$t_{\text{QVWX}}$	5	–	$t_{\text{CLCL}} - 37$	–	ns
Data setup before $\overline{\text{WR}}$	$t_{\text{QVWH}}$	170	–	$7 t_{\text{CLCL}} - 122$	–	ns
Data hold after $\overline{\text{WR}}$	$t_{\text{WHQX}}$	15	–	$t_{\text{CLCL}} - 27$	–	ns
Address float after $\overline{\text{RD}}$	$t_{\text{RLAZ}}$	–	0	–	0	ns

## AC Characteristics for C501-L24 / C501-1R24 (cont'd)

### External Clock Drive Characteristics

Parameter	Symbol	Limit Values		Unit
		Variable Clock Freq. = 3.5 MHz to 24 MHz		
		min.	max.	
Oscillator period	$t_{CLCL}$	41.7	285.7	ns
High time	$t_{CHCX}$	12	$t_{CLCL} - t_{CLCX}$	ns
Low time	$t_{CLCX}$	12	$t_{CLCL} - t_{CHCX}$	ns
Rise time	$t_{CLCH}$	–	12	ns
Fall time	$t_{CHCL}$	–	12	ns

## AC Characteristics for C501-L40 / C501-1R40

$V_{CC} = 5\text{ V} + 10\%, -15\%$ ;  $V_{SS} = 0\text{ V}$

$T_A = 0\text{ °C to }70\text{ °C}$  for the SAB-C501

$T_A = -40\text{ °C to }85\text{ °C}$  for the SAF-C501

( $C_L$  for port 0, ALE and  $\overline{\text{PSEN}}$  outputs = 100 pF;  $C_L$  for all other outputs = 80 pF)

## Program Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		40 MHz Clock		Variable Clock $1/t_{\text{CLCL}} = 3.5\text{ MHz to }40\text{ MHz}$		
		min.	max.	min.	max.	
ALE pulse width	$t_{\text{LHLL}}$	35	–	$2 t_{\text{CLCL}} - 15$	–	ns
Address setup to ALE	$t_{\text{AVLL}}$	10	–	$t_{\text{CLCL}} - 15$	–	ns
Address hold after ALE	$t_{\text{LLAX}}$	10	–	$t_{\text{CLCL}} - 15$	–	ns
ALE low to valid instr in	$t_{\text{LLIV}}$	–	55	–	$4 t_{\text{CLCL}} - 45$	ns
ALE to $\overline{\text{PSEN}}$	$t_{\text{LLPL}}$	10	–	$t_{\text{CLCL}} - 15$	–	ns
$\overline{\text{PSEN}}$ pulse width	$t_{\text{PLPH}}$	60	–	$3 t_{\text{CLCL}} - 15$	–	ns
$\overline{\text{PSEN}}$ to valid instr in	$t_{\text{PLIV}}$	–	25	–	$3 t_{\text{CLCL}} - 50$	ns
Input instruction hold after $\overline{\text{PSEN}}$	$t_{\text{PXIX}}$	0	–	0	–	ns
Input instruction float after $\overline{\text{PSEN}}$	$t_{\text{PXIZ}}^*)$	–	20	–	$t_{\text{CLCL}} - 5$	ns
Address valid after $\overline{\text{PSEN}}$	$t_{\text{PXAV}}^*)$	20	–	$t_{\text{CLCL}} - 5$	–	ns
Address to valid instr in	$t_{\text{AVIV}}$	–	65	–	$5 t_{\text{CLCL}} - 60$	ns
Address float to $\overline{\text{PSEN}}$	$t_{\text{AZPL}}$	– 5	–	– 5	–	ns

\*) Interfacing the C501 to devices with float times up to 25 ns is permissible. This limited bus contention will not cause any damage to port 0 Drivers.

## AC Characteristics for C501-L40 / C501-1R40 (cont'd)

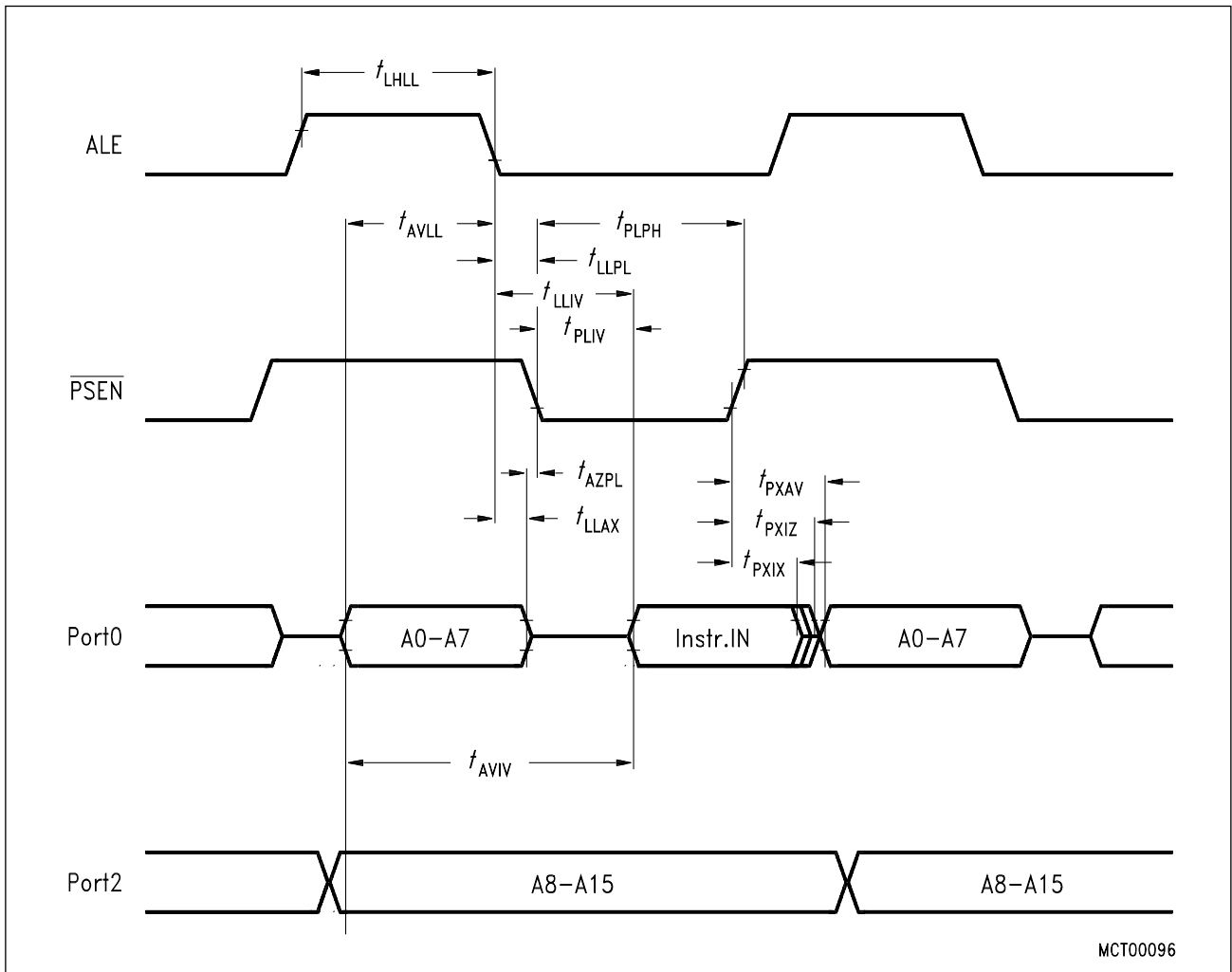
### External Data Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		40 MHz Clock		Variable Clock $1/t_{\text{CLCL}} = 3.5 \text{ MHz to } 40 \text{ MHz}$		
		min.	max.	min.	max.	
$\overline{\text{RD}}$ pulse width	$t_{\text{RLRH}}$	120	–	$6 t_{\text{CLCL}} - 30$	–	ns
$\overline{\text{WR}}$ pulse width	$t_{\text{WLWH}}$	120	–	$6 t_{\text{CLCL}} - 30$	–	ns
Address hold after ALE	$t_{\text{LLAX2}}$	10	–	$t_{\text{CLCL}} - 15$	–	ns
$\overline{\text{RD}}$ to valid data in	$t_{\text{RLDV}}$	–	75	–	$5 t_{\text{CLCL}} - 50$	ns
Data hold after $\overline{\text{RD}}$	$t_{\text{RHDX}}$	0	–	0	–	ns
Data float after $\overline{\text{RD}}$	$t_{\text{RHDZ}}$	–	38	–	$2 t_{\text{CLCL}} - 12$	ns
ALE to valid data in	$t_{\text{LLDV}}$	–	150	–	$8 t_{\text{CLCL}} - 50$	ns
Address to valid data in	$t_{\text{AVDV}}$	–	150	–	$9 t_{\text{CLCL}} - 75$	ns
ALE to $\overline{\text{WR}}$ or $\overline{\text{RD}}$	$t_{\text{LLWL}}$	60	90	$3 t_{\text{CLCL}} - 15$	$3 t_{\text{CLCL}} + 15$	ns
Address valid to $\overline{\text{WR}}$ or $\overline{\text{RD}}$	$t_{\text{AVWL}}$	70	–	$4 t_{\text{CLCL}} - 30$	–	ns
$\overline{\text{WR}}$ or $\overline{\text{RD}}$ high to ALE high	$t_{\text{WHLH}}$	10	40	$t_{\text{CLCL}} - 15$	$t_{\text{CLCL}} + 15$	ns
Data valid to $\overline{\text{WR}}$ transition	$t_{\text{QVWX}}$	5	–	$t_{\text{CLCL}} - 20$	–	ns
Data setup before $\overline{\text{WR}}$	$t_{\text{QVWH}}$	125	–	$7 t_{\text{CLCL}} - 50$	–	ns
Data hold after $\overline{\text{WR}}$	$t_{\text{WHQX}}$	5	–	$t_{\text{CLCL}} - 20$	–	ns
Address float after $\overline{\text{RD}}$	$t_{\text{RLAZ}}$	–	0	–	0	ns

## AC Characteristics for C501-L40 / C501-1R40 (cont'd)

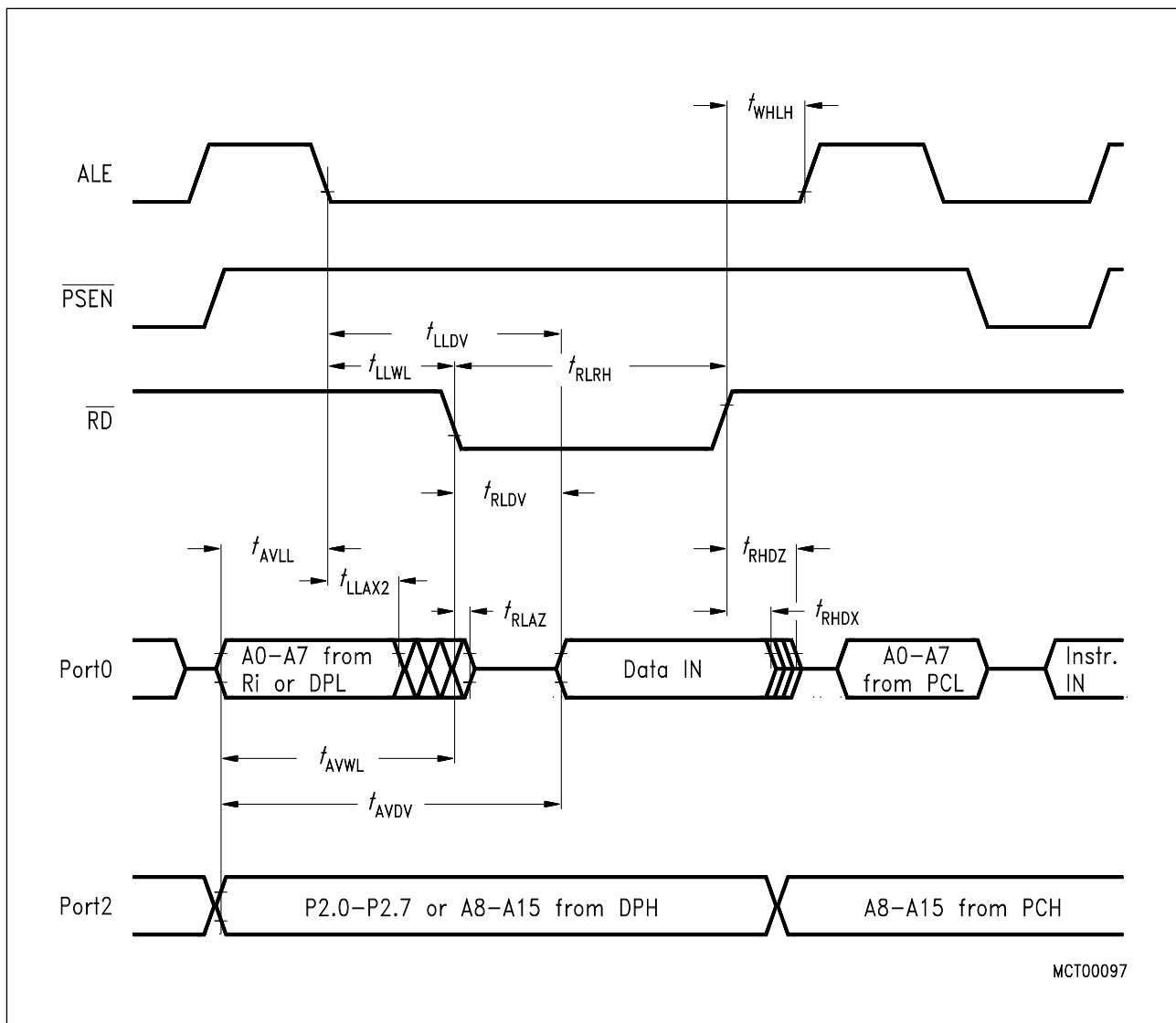
### External Clock Drive Characteristics

Parameter	Symbol	Limit Values		Unit
		Variable Clock Freq. = 3.5 MHz to 40 MHz		
		min.	max.	
Oscillator period	$t_{CLCL}$	25	285.7	ns
High time	$t_{CHCX}$	10	$t_{CLCL} - t_{CLCX}$	ns
Low time	$t_{CLCX}$	10	$t_{CLCL} - t_{CHCX}$	ns
Rise time	$t_{CLCH}$	–	10	ns
Fall time	$t_{CHCL}$	–	10	ns

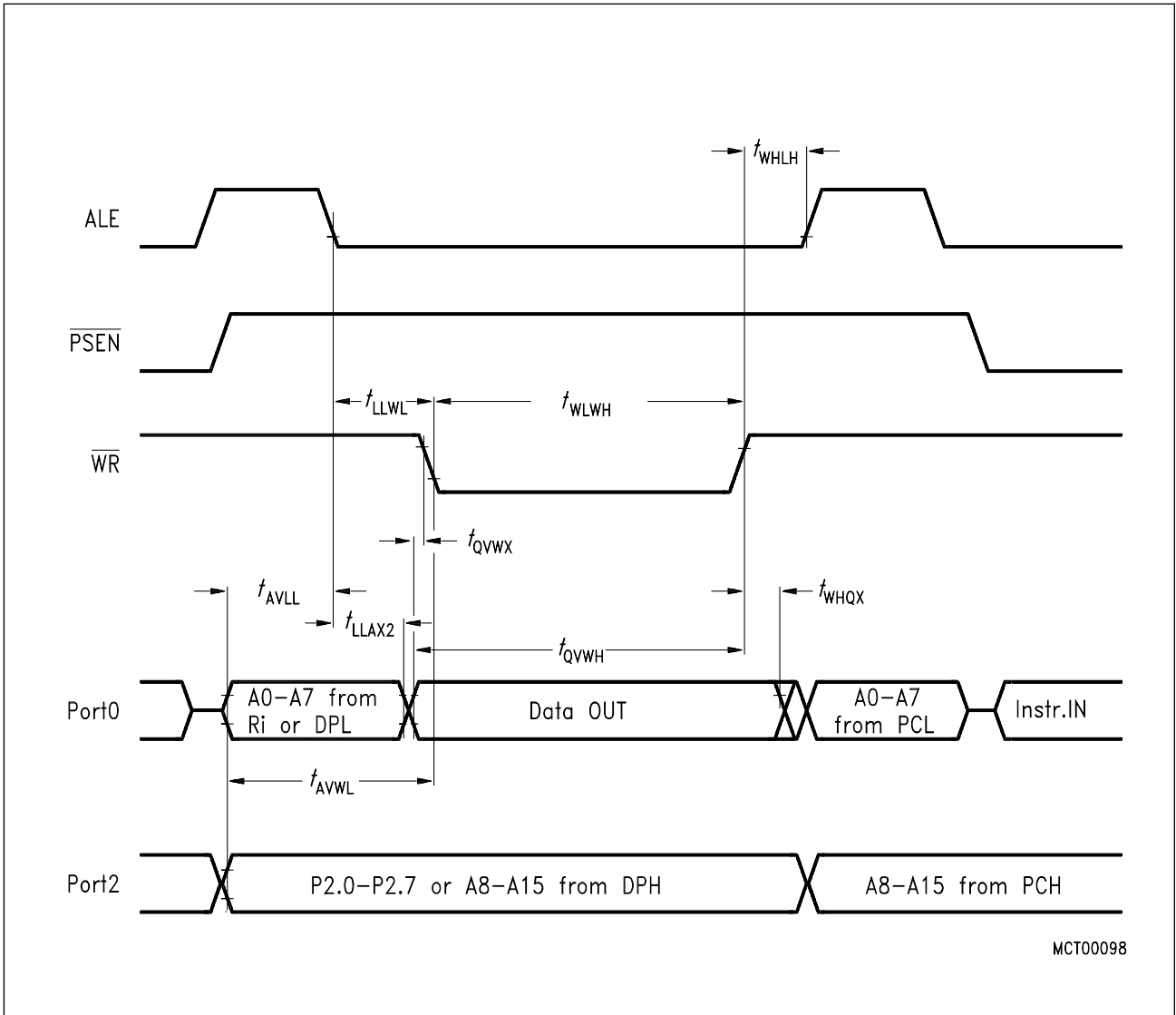


MCT00096

**Figure 4**  
Program Memory Read Cycle



**Figure 5**  
**Data Memory Read Cycle**

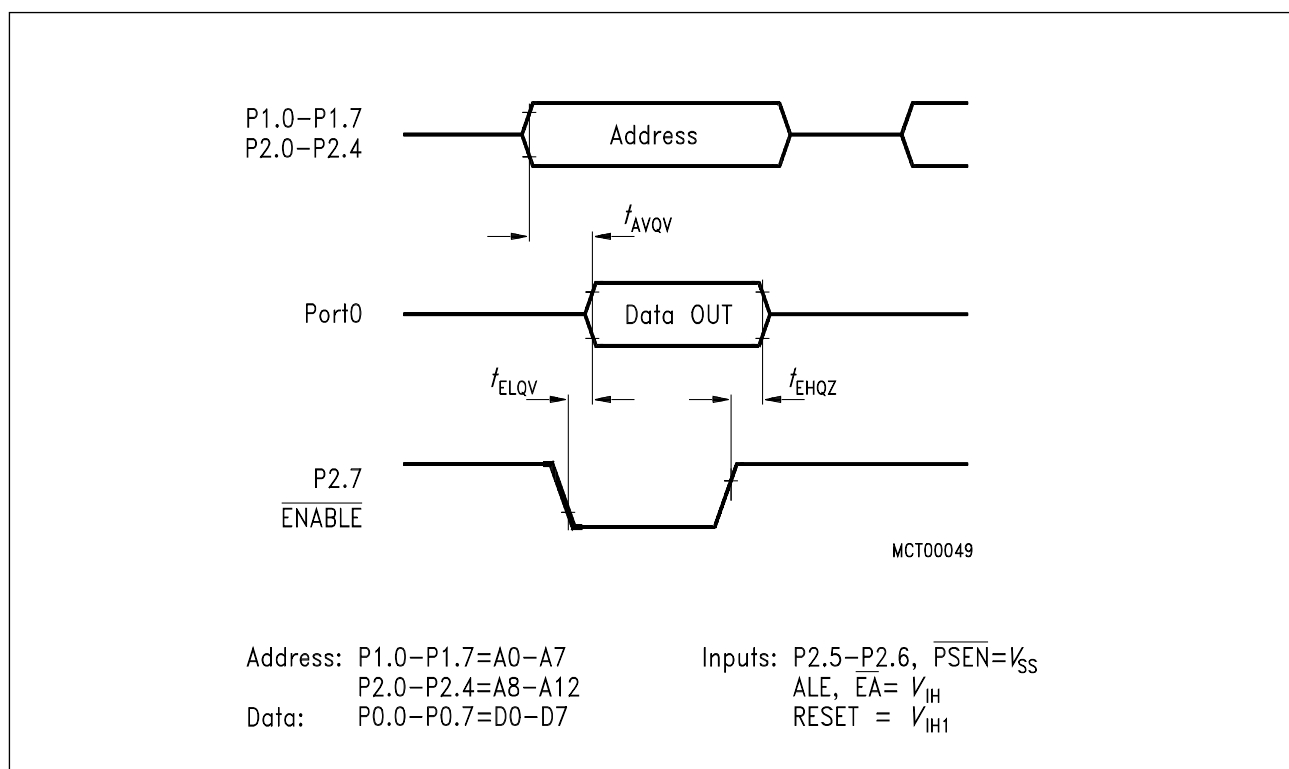


**Figure 6**  
**Data Memory Write Cycle**

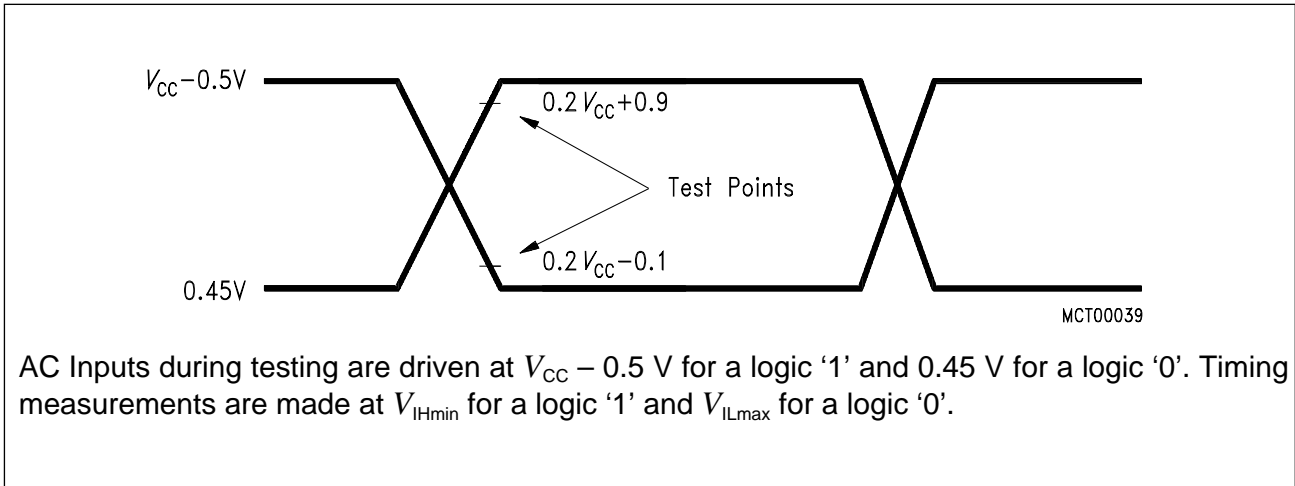
## ROM Verification Characteristics for C501-1R

### ROM Verification Mode 1

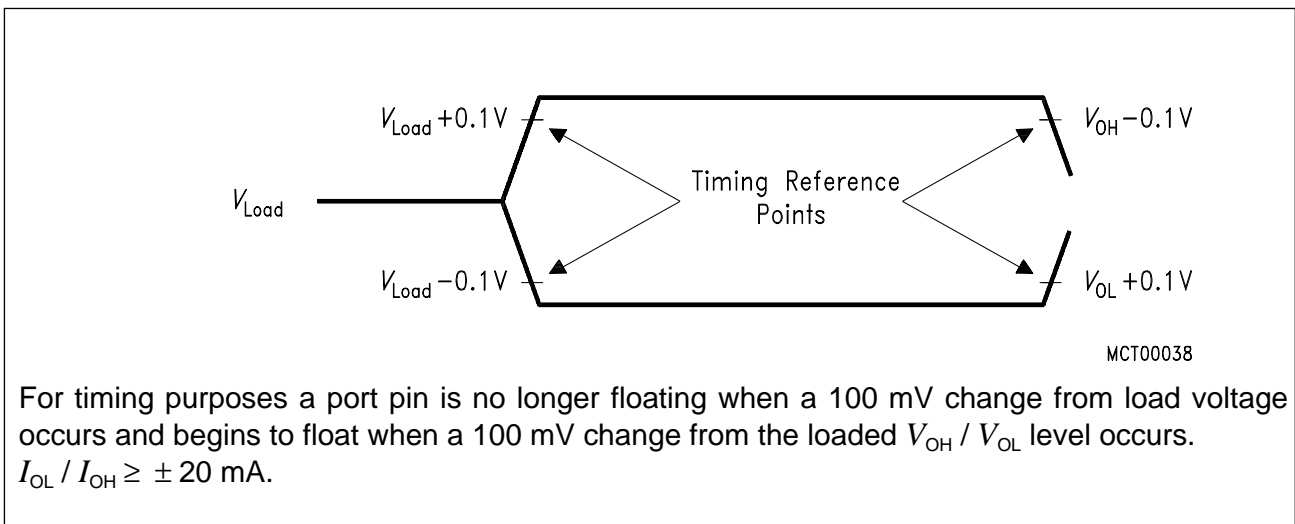
Parameter	Symbol	Limit Values		Unit
		min.	max.	
Address to valid data	$t_{AVQV}$	—	$48 t_{CLCL}$	ns
ENABLE to valid data	$t_{ELQV}$	—	$48 t_{CLCL}$	ns
Data float after ENABLE	$t_{EHQZ}$	0	$48 t_{CLCL}$	ns
Oscillator frequency	$1/t_{CLCL}$	4	6	MHz



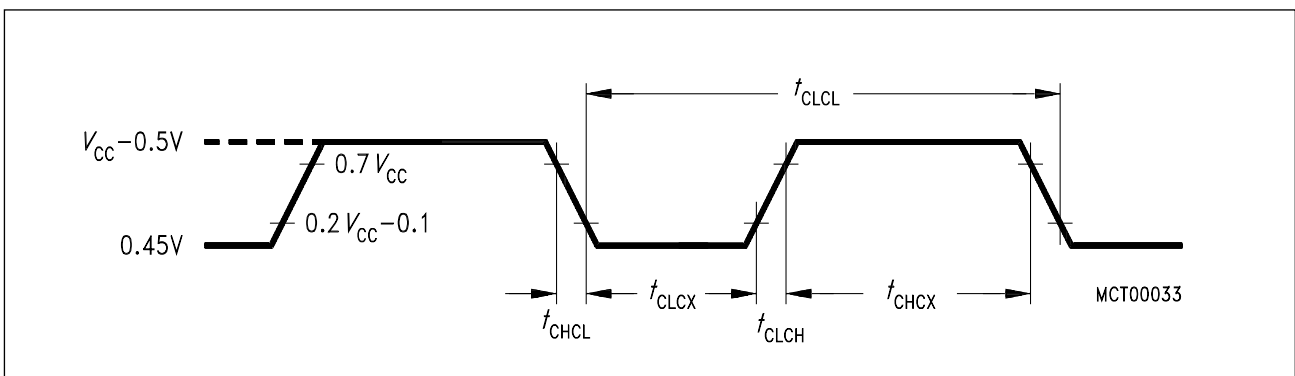
**Figure 7**  
**ROM Verification Mode 1**



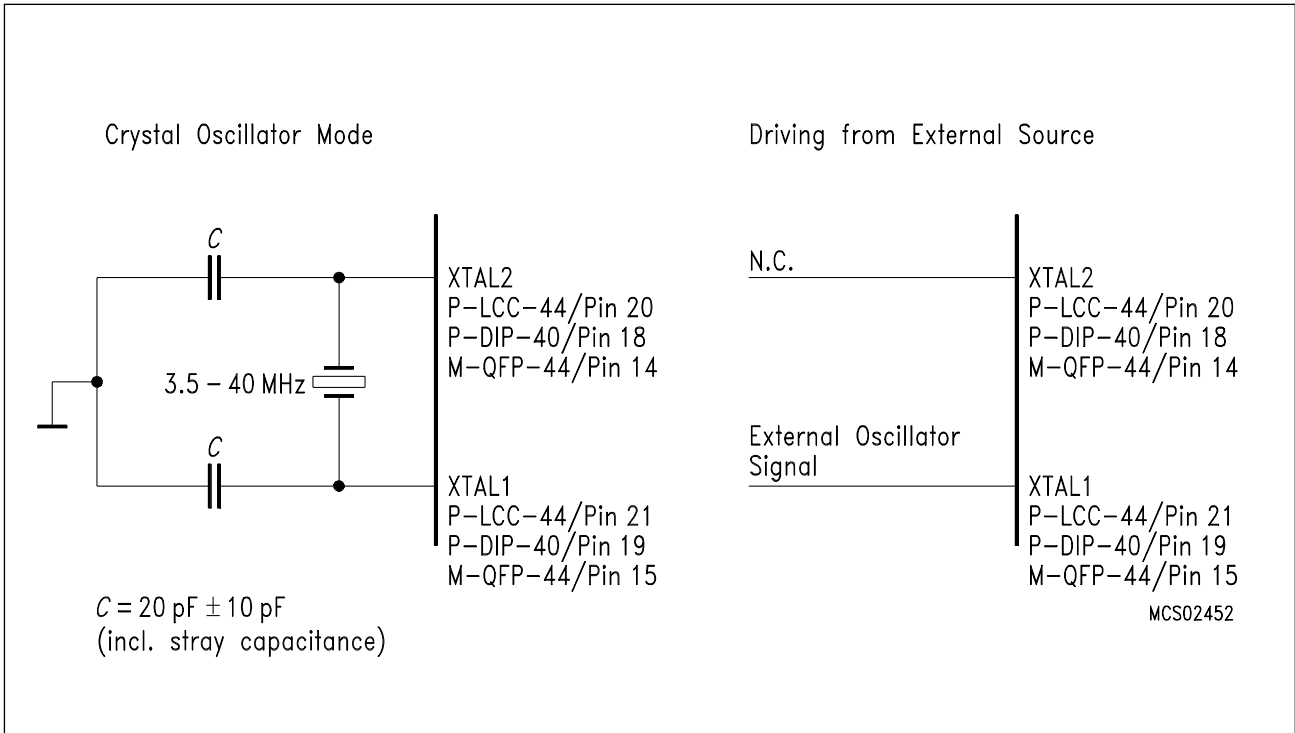
**Figure 8**  
AC Testing: Input, Output Waveforms



**Figure 9**  
AC Testing: Float Waveforms



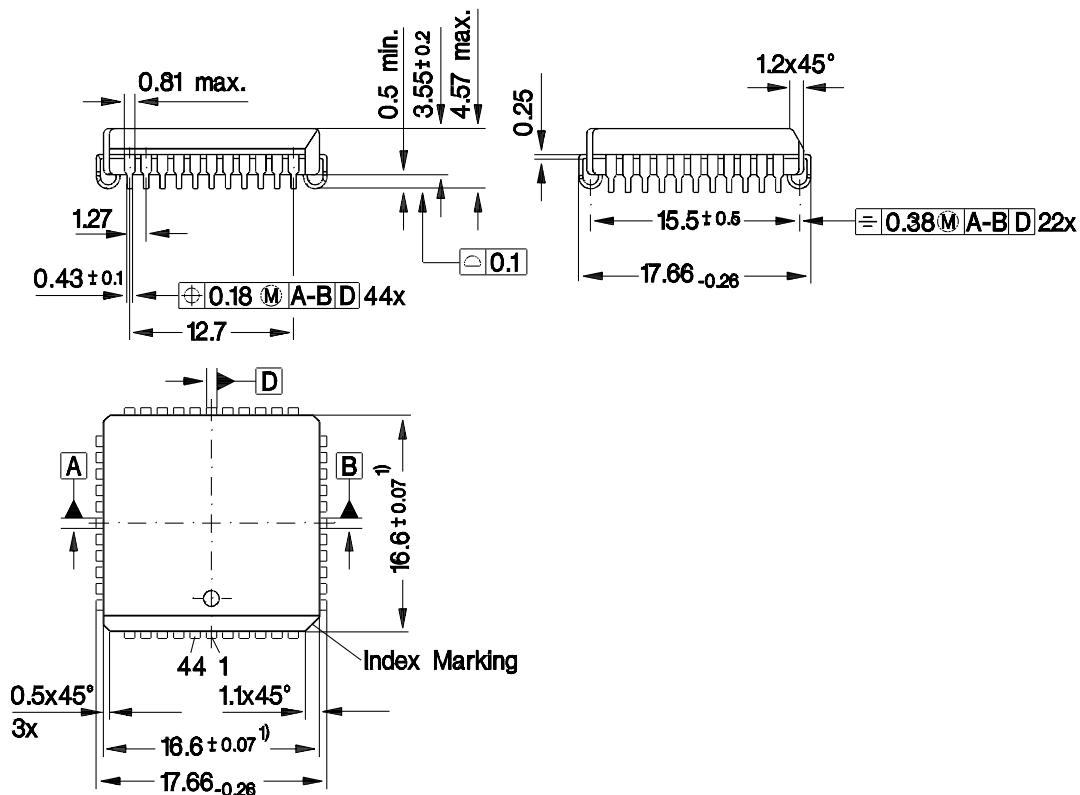
**Figure 10**  
External Clock Cycle



**Figure 11**  
**Recommended Oscillator Circuits**

## Package Outlines

### P-LCC-44 – SMD for C501-L / C501-1R (“non-G“ Versions) (Plastic Leaded Chip-Carrier)



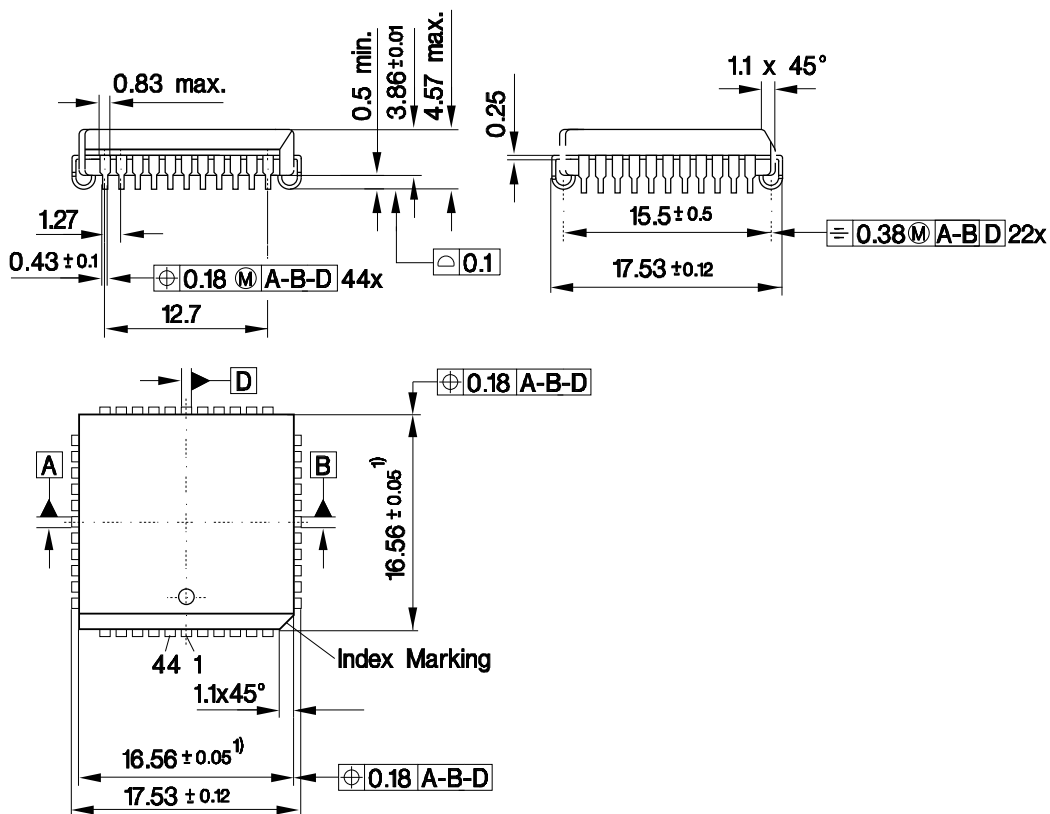
### Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”

SMD = Surface Mounted Device

Dimensions in mm

**P-LCC-44 – SMD for C501G-L / C501G-1R (“G” Versions)**  
 (Plastic Leaded Chip-Carrier)



1) Does not include plastic or metal protrusion of 0.15 max. per side

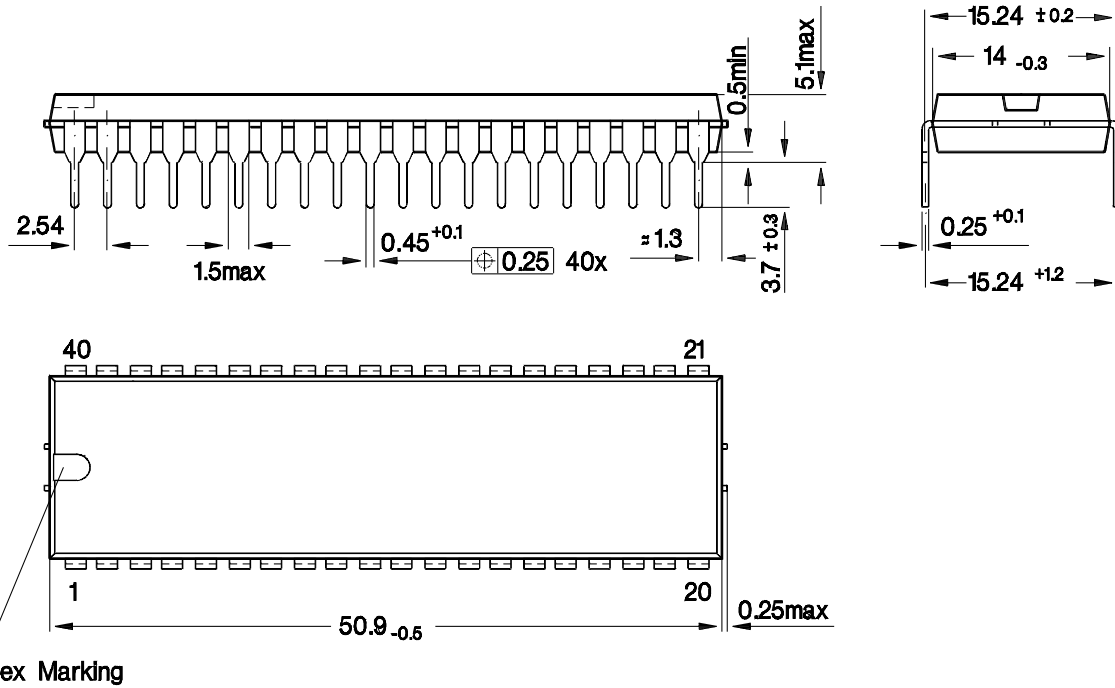
**Sorts of Packing**

Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”

SMD = Surface Mounted Device

Dimensions in mm

**P-DIP-40 for C501-L / C501-1R (“non-G” Versions)**  
 (Plastic Dual in-Line Package)



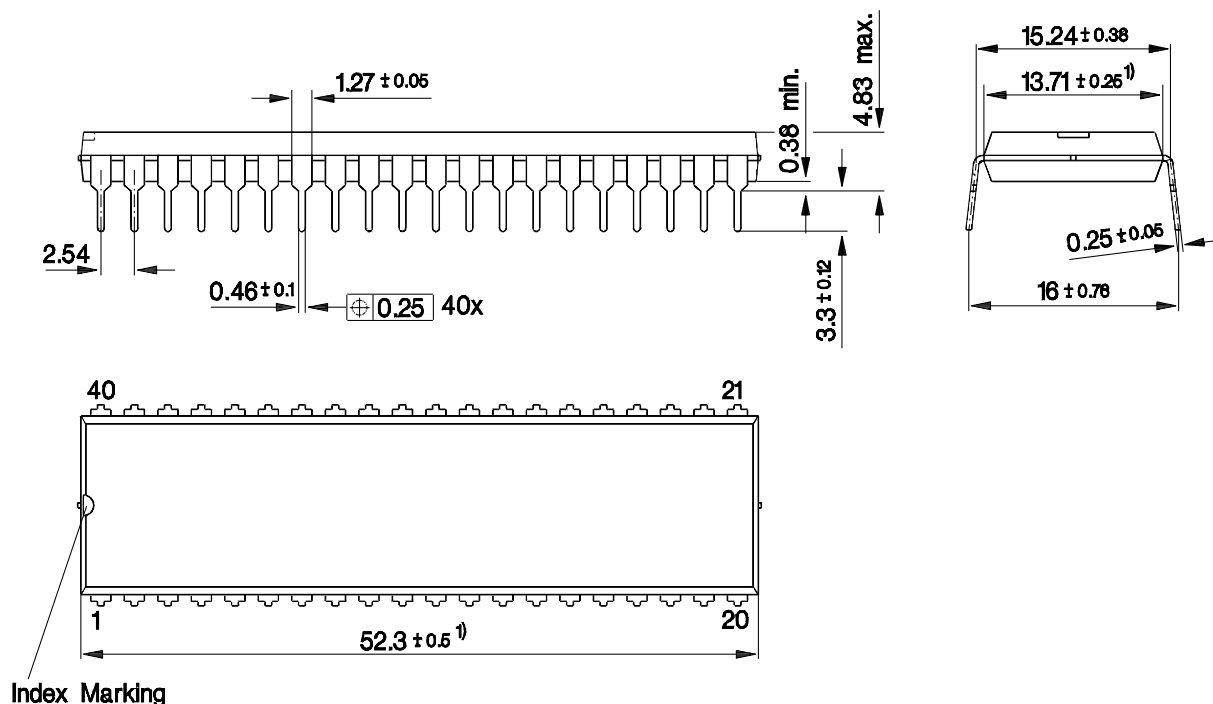
**Sorts of Packing**

Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”

SMD = Surface Mounted Device

Dimensions in mm

**P-DIP-40 for C501G-L / C501G-1R (“G” Versions)**  
 (Plastic Dual in-Line Package)



1) Does not include plastic or metal protrusion of 0.25 max. per side

**Sorts of Packing**

Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”

SMD = Surface Mounted Device

Dimensions in mm



**P-MQFP-44 – SMD for C501G-L / C501G-1R (“G” Versions)**  
(Plastic Metric Quad Flat Package)

Detailed schematic is to be defined

**Sorts of Packing**

Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”

SMD = Surface Mounted Device

Dimensions in mm